DATA SHEET

旭曜科技
ORISE TECH



# OTM3206A

## 720-channel 6-bit Source Driver with System-on-chip for Color Amorphous TFT-LCDs

***Preliminary***

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# 720-CHANNEL DRIVER WITH SYSTEM-ON-CHIP (SOC) FOR COLOR AMORPHOUS TFT LCD

## 1. GENERAL DESCRIPTION

The OTM3206A, a 262144-color System-on-Chip (SoC) driver LSI designed for small and medium sizes of TFT LCD display, is capable of supporting up to 240xRGBx320 in resolution which can be achieved by the designated RAM for graphic data. The 396-channel source driver has true 6-bit resolution, which generates 64 Gamma-corrected values by an internal D/A converter.

The OTM3206A is able to operate with low IO interface power supply up to 1.6V and incorporate with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and source driver.

The built-in timing controller in OTM3206A can support several interfaces for the diverse request of medium or small size portable display. OTM3206A provides system interfaces, which include 8-/9-/16-/18-bit parallel interfaces and serial interface (SPI), to configure system. Not only can the system interfaces be used to configure system, they can also access RAM at high speed for still picture display. The OTM3206A also supports a function to display eight colors and a standby mode for power control consideration.

## 2. FEATURES

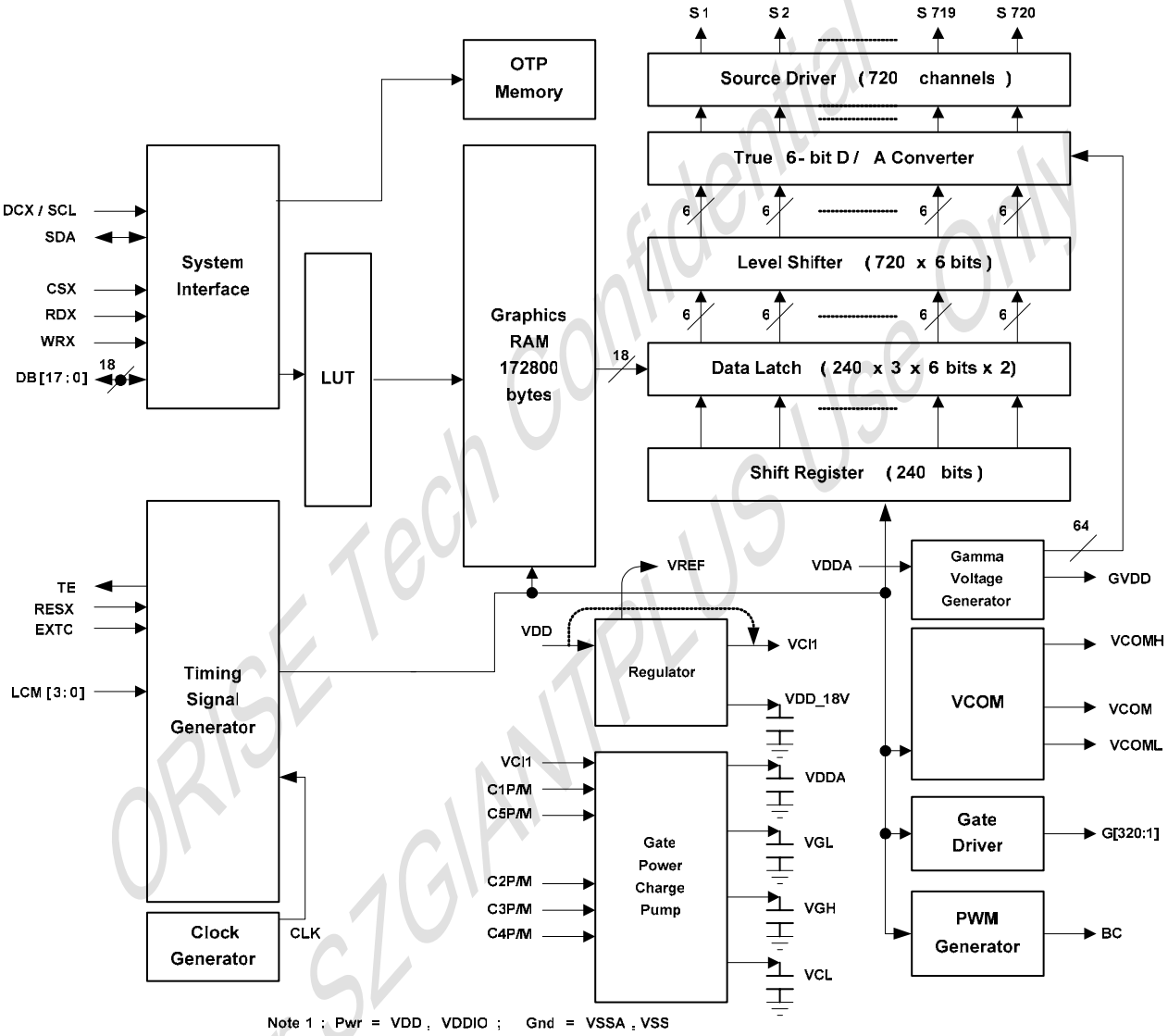
- One-chip solution for amorphous TFT-LCD.
- Supports resolution up to 240xRGBx320, incorporating a 720-channel source driver and a 320-channel gate driver
- Outputs 64 $\gamma$ -corrected values using an internal true 6-bit resolution D/A converter to achieve 262K colors
- Built-in 172800 bytes internal RAM
- Line Inversion AC drive / frame inversion AC drive
- System interfaces
  - High-speed interfaces to 8-, 9-, 16-, and 18-bit parallel ports
  - 3-pin 9 bits or 4-pin 8 bits Serial Peripheral Interface (SPI)
- Diverse RAM accessing for functional display
  - Window address function to display at any area on the screen via a moving picture display interface
  - Window address function to limit the data rewriting area and reduce data transfer
  - Moving and still picture can display at the same time
  - Vertical scrolling function
  - Partial screen display
- Power supply
  - Logic power supply voltage (VDD): 2.5 ~ 3.6 V
  - I/O interface supply voltage (VDDIO): 1.6 ~ 3.6 V
  - Analog power supply voltage (VDD): 2.5 ~ 3.6V
- On-chip power management system
  - Power saving mode (standby / 8-color mode, etc)
  - Low power consumption structure for source driver.
- Built-in Charge Pump circuits
  - Source driver voltage level : 2 times (x2) of Vci1
  - Gate driver voltage level (VGH, VGL) up to 6 times (x6) and minus 5 times (x-5) Vci1
- Built-in internal oscillator and hardware reset
- Built–in One-Time-Programming (OTP) function for VCOM amplitude and VcomH voltage adjustment.

## 3. ORDERING INFORMATION

| Product Number | Package Type |
|---|---|
| OTM3206A-C | Chip Form With Gold Bump |

## 4. BLOCK DIAGRAM

### 4.1. Block Function



#### 4.1.1. System Interface

The OTM3206A supports three high-speed system interfaces:

1. 80-system high-speed interfaces with 8-, 9-, 16-, 18-bit parallel ports.
2. 68-system high-speed interfaces with 8-, 9-, 16-, 18-bit parallel ports.
3. 3-pin 9-bits or 4-pin 8 bits Serial Peripheral Interface (SPI).

The OTM3206A has a 16-bit index register (IR) and two 18-bit data registers, a write-data register (WDR) and a read-data register (RDR). The IR register is used to store index information from control registers. The WDR register is used to temporarily store data to be written for register control and internal GRAM. The RDR register is used to temporarily store data read from the GRAM. When graphic data is written to the internal GRAM from MCU/graphic engine, the data is first written to the WDR and then automatically written to the internal GRAM in internal operation. When graphic data read operation is executed, graphic data is read via the RDR from the internal GRAM. Therefore, invalid data is first read out to the data bus when the OTM3206A executes the 1st read operation. Thus, valid data can be read out after the OTM3206A executes the 2nd read operation.

#### 4.1.2. Address Counter (AC)

OTM3206A features an Address Counter (AC) giving an address to the internal GRAM. The address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

#### 4.1.3. Graphics RAM (GRAM)

OTM3206A features a 172800-byte (320 x 240x 18 / 8) Graphic RAM (GRAM).

#### 4.1.4. Grayscale Voltage Generating Circuit

OTM3206A has true 6-bit resolution D/A converter, which generates 64 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ-correction register.

#### 4.1.5. Timing Controller

OTM3206A has a timing controller, which can generate a timing signal for internal circuit operation such as gate output timing, RAM accessing timing, etc.

#### 4.1.6. Oscillator (OSC)

The OTM3206A also features an internal oscillator to generate RC oscillation with an internal resistor. In standby mode, RC oscillation is halted to reduce power consumption.

#### 4.1.7. Source Driver Circuit

OTM3206A consists of a 720-output source driver circuit (S1 ~ S720). Data in the GRAM are latched when the 396th bit data is input. The latched data controls the source driver and generates a drive waveform.

#### 4.1.8. Gate Driver Circuit

OTM3206A consists of a 320-output gate driver circuit (G1~G320). The gate driver circuit outputs gate driver signals at either VGH or VGL level.

#### 4.1.9. LCD Driving Power Supply Circuit

The LCD driving power supply circuit generates the voltage levels AVDD, VGH, VGL and VCOM for driving an LCD. All this voltages can be adjusted by register setting.

## 5. SIGNAL DESCRIPTIONS

<table>
<tr><th>Signal</th><th>I/O</th><th>Connected with</th><th>Function</th></tr>
<tr><td colspan="4">System Configuration Input Signal</td></tr>
<tr><td>IM3~0,</td><td>I</td><td>VSS/ VDDIO</td><td>Select system interface mode.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th></th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 8-bits Parallel interface</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 9-bits Parallel interface</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 16-bits Parallel interface</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 18-bits Parallel interface</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>6800 MCU 8-bits Parallel interface</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6800 MCU 9-bits Parallel interface</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>6800 MCU 16-bits Parallel interface</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>6800 MCU 18-bits Parallel interface</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>3-Pin Serial interface</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>4-Pin Serial interface</td></tr>
</table></td></tr>
<tr><td>RESX</td><td>I</td><td>MPU or<br>external<br>RC circuit</td><td>Reset pin. This is an active low signal.</td></tr>
<tr><td>EXTC</td><td>1</td><td>VSS/ VDDIO</td><td>Extend command set access<br>Low: Extend command set is not accessible.<br>High: Extend command set is accessible.<br>If this is not used. Open it (This pin is internally pull low).</td></tr>
<tr><td colspan="4">Interface input Signals</td></tr>
<tr><td>CSX</td><td>I</td><td>MPU</td><td>Chip select signal.<br>Low: the OTM3206A is accessible<br>High: the OTM3206A is not accessible<br>This pin has can be permanently fixed “Low” in MCU interface mode only.</td></tr>
<tr><td>D/CX<br>(SCL)</td><td>I</td><td>MPU</td><td>Display data / Command selection pin in parallel interface<br>Low: Command data<br>High: Display data<br>In SPI I/F, this is used as SCL pin.<br>Must connect to the VSS or VDDIO level when not used.</td></tr>
<tr><td>WRX<br>(R/WX)</td><td>I</td><td>MPU</td><td>(A) In 80-system interface mode, a write strobe signal can be input via this pin and initializes a write operation when the signal is low.<br>(B) In 68-system interface mode, a write or read control signal can be input via this pin and initializes a write or read operation.<br>Must connect to the VSS or VDDIO level when not used.</td></tr>
<tr><td>RDX<br>(E)</td><td>I</td><td>MPU</td><td>In 80-system interface mode, a read strobe signal can be input via this pin and initializes a read operation when the signal is low.<br>In 68system interface mode, a strobe signal can be input via this pin and initializes a write or read operation when the signal is low.<br>Must connect to the VSS or VDDIO level when not in use.</td></tr>
<tr><td>DB0-DB17</td><td>I/O</td><td>MPU</td><td>(A) When MCU I/F,<br>D[17:0] are used to MCU parallel interface data bus<br>(B) In SPI I/F, D0 is used as Serial input/ output signal.(SDA)</td></tr>
</table>

| Signal | I/O | Connected with | Function |
|---|---|---|---|
| | | | In SPI I/F, D[17:1] not used, please fix this pin at VDDIO or VSS level. |
| **Charge Pump and Power Supply Signal** | | | |
| C1P/M, C2P/M C3P/M, C4P/M C5P/M | - | Step-up capacitor | Connect boost capacitors for the internal DC/DC converter circuit to these pins. Leave the pins open when DC/DC converter circuits are not used. |
| VDDA | O | Stabilizing capacitor | Output 2x VCI1 voltage level from the step-up circuit 1. Place a stabilizing capacitor between VSS. AVDD = 4.5 ~ 5.5V |
| VGH | O | Stabilizing capacitor | An output voltage from the step-up circuit 2x, 4x ~ 6x of the VCI1 level. Connect with a stabilizing capacitor. |
| VGL | O | Stabilizing capacitor | An output voltage from the step-up circuit –2x, -3x ~ -5x of the VCI1 level. Connect with a stabilizing capacitor. |
| VCL | O | Stabilizing capacitor | An output voltage from the step-up circuit 2, –1x of the VCI1 level. Connect with a stabilizing capacitor. |
| VDD_18V | O | Stabilizing capacitor | Reference voltage for Internal logic block Connect with a stabilizing capacitor |
| VCI1 | O | | An internal reference voltage level, which is regulated from VDD. The amplitude of VCI1 is from VDD-VSS. |
| VREF | O | | Reference voltage for power block |
| GVDD | O | | Output source driver grayscale reference voltage level. |
| **Source/Gate Driver and VCOM Signals** | | | |
| G1~G320 | O | LCD | Output gate driver signals, which has the swing from VGH to VGL |
| S1~S720 | O | LCD | Output source driver signals. The D/A converted 64-gray-scale analog voltage is output. |
| VCOM | O | TFT panel common electrode | Output a square wave signal with the swing from VcomH - VcomL to the common electrode of TFT panel. The alternating cycle can be set to frame inversion or 1-line inversion. |
| VcomH | O | Stabilizing Capacitor or open. | Output the high level of VCOM voltage. |
| VcomL | O | Stabilizing capacitor or open | Output the low level of VCOM voltage. |
| VDDIO | I | Stabilizing capacitor or open. | VDDIO input voltage for control pins using |
| VDD | I | | Power supply Input |
| VDD_BC | I | | Power supply input. |
| VSS | | | Digital ground pin. |
| VSSA | | | Analog ground pin. |
| **Misc. Signal** | | | |
| TE | O | MPU | Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command. When this pin is not activated (TE function OFF), this pin is VSS level. |

| Signal | I/O | Connected with | Function |
|---|---|---|---|
| VDD_OTP | I | | OTP external power supply,. |
| TEST1-12 | T | | Test pin. If not used, please open this pin. |
| Dummy1~12 | D | | Dummy pin. please open this pin. |
| BC | O | | PWM ouput. |

## 6. INSTRUCTIONS

### 6.1. Outline

The OTM3206A supports 18-bit data bus interface to configure system via accessing command register. When the command register is executed, sending the command information to specify which index register would be accessed and following the data to that control register. Moreover, register accessing operation should cooperate with DC/X, WRX, RDX signal for OTM3206A to recognize the control instruction. And command instruction can be accomplished using all system interfaces (18-bit, 16-bit, 9-bit, 8-bit 80- or 68-system and SPI)..

### 6.1.1. System Function Command List and Description

Table 6.1.1 list all the system function command. After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section). Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTR (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh) and Read Display Self Diagnostic Result (0Fh) of these commands are updated immediately both in Sleep In mode and Sleep Out mode.

Table 6.1.1 System Function command List (1)

| Instruction | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Hex) | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NOP | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | (00h) | No Operation |
| SWRESET | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (01h) | Software reset |
| RDDID | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | (04h) | Read Display ID |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | | Dummy read |
| | 1 | 1 | ↑ | - | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | | ID1 read |
| | 1 | 1 | ↑ | - | ID27 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 | | ID2 read |
| | 1 | 1 | ↑ | - | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 | | ID3 read |
| RDDST | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | (09h) | Read Display Status |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | | Dummy read |
| | 1 | 1 | ↑ | - | BSTON | MY | MX | MV | ML | RGB | MH | ST24 | | - |
| | 1 | 1 | ↑ | - | ST23 | IFPF2 | IFPF1 | IFPF0 | IDMON | PTLON | SLOUT | NORON | | - |
| | 1 | 1 | ↑ | - | VSSON | ST14 | INVON | ST12 | ST11 | DISON | TEON | GCS2 | | - |
| | 1 | 1 | ↑ | - | GCS1 | GCS0 | TELOM | HSON | VSON | PCKON | DEON | ST0 | | - |
| RDDPM | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | (0Ah) | Read Display Power Mode |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | | Dummy read |
| | 1 | 1 | ↑ | - | BSTON | IDMON | PTLON | SLPOUT | NORON | DISON | D1 | D0 | | - |
| RDD MADCTR | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | (0Bh) | Read Display MADCTR |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | | Dummy read |
| | 1 | 1 | ↑ | - | MX | MY | MV | ML | RGB | MH | D1 | D0 | | - |
| RDD COLMOD | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | (0Ch) | Read Display Pixel Format |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | | Dummy read |
| | 1 | 1 | ↑ | - | D7 | D6 | D5 | D4 | D3 | IFPF2 | IFPF1 | IFPF0 | | - |
| RDDIM | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | (0Dh) | Read Display Image Mode |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | | Dummy read |
| | 1 | 1 | ↑ | - | VSSON | D6 | INVON | D4 | D3 | GCS2 | GCS1 | GCS0 | | - |
| RDDSM | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | (0Eh) | Read Display Signal Mode |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | | Dummy read |
| | 1 | 1 | ↑ | - | TEON | TELOM | HSON | VSON | PCKON | DEON | D1 | D0 | | - |
| RDDSDR | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | (0Fh) | Read Display Self-diagnostic result |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | | Dummy read |
| | 1 | 1 | ↑ | - | RELD | FUND | D5 | D4 | D3 | D2 | D1 | D0 | | - |

"-": Don't care, can be set to VDDIO or VSS level

Table 6.1.1 System Function command List (2)

| Instruction | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Hex) | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SLPIN | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | (10h) | Sleep in & booster off |
| SLPOUT | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | (11h) | Sleep out & booster on |
| PTLON | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | (12h) | Partial mode on |
| NORON | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | (13h) | Partial off (Normal) |
| INVOFF | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | (20h) | Display inversion off (normal) |
| INVON | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | (21h) | Display inversion on |
| GAMSET | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | (26h) | Gamma curve select |
| | 1 | ↑ | 1 | - | GC7 | GC6 | GC5 | GC4 | GC3 | GC2 | GC1 | GC0 | | - |
| DISPOFF | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | (28h) | Display off |
| DISPON | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | (29h) | Display on |
| CASET | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | (2Ah) | Column address set |
| | 1 | ↑ | 1 | - | XS15 | XS14 | XS13 | XS12 | XS11 | XS10 | XS9 | XS8 | | X address start: 0 ≤ XS ≤ 0xEF |
| | 1 | ↑ | 1 | - | XS7 | XS6 | XS5 | XS4 | XS3 | XS2 | XS1 | XS0 | | |
| | 1 | ↑ | 1 | - | XE15 | XE14 | XE13 | XE12 | XE11 | XE10 | XE9 | XE8 | | X address end: XS ≤ XE ≤ 0xEF |
| | 1 | ↑ | 1 | - | XE7 | XE6 | XE5 | XE4 | XE3 | XE2 | XE1 | XE0 | | |
| RASET | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | (2Bh) | Row address set |
| | 1 | ↑ | 1 | - | YS15 | YS14 | YS13 | YS12 | YS11 | YS10 | YS9 | YS8 | | Y address start: 0 ≤ YS ≤ 0x13F |
| | 1 | ↑ | 1 | - | YS7 | YS6 | YS5 | YS4 | YS3 | YS2 | YS1 | YS0 | | |
| | 1 | ↑ | 1 | - | YE15 | YE14 | YE13 | YE12 | YE11 | YE10 | YE9 | YE8 | | Y address end: YS ≤ YE ≤ 0x13F |
| | 1 | ↑ | 1 | - | YE7 | YE6 | YE5 | YE4 | YE3 | YE2 | YE1 | YE0 | | |
| RAMWR | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | (2Ch) | Memory write |
| | 1 | ↑ | 1 | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | Write data |
| RAMHD | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | (2Eh) | Memory read |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | | Dummy read |
| | 1 | 1 | ↑ | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | Read data |

"-": Don't care, can be set to VDDIO or VSS level

Table 6.1.1 System Function command List (3)

| Instruction | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Hex) | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PTLAR | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | (30h) | Partial start/end address set |
| | 1 | ↑ | 1 | - | PSL15 | PSL14 | PSL13 | PSL12 | PSL11 | PSL10 | PSL9 | PSL8 | | Partial start address (0,1,2, .., 319) |
| | 1 | ↑ | 1 | - | PSL7 | PSL6 | PSL5 | PSL4 | PSL3 | PSL2 | PSL1 | PSL0 | | |
| | 1 | ↑ | 1 | - | PEL15 | PEL14 | PEL13 | PEL12 | PEL11 | PEL10 | PEL9 | PEL8 | | Partial end address (0,1,2, .., 319) |
| | 1 | ↑ | 1 | - | PEL7 | PEL6 | PEL5 | PEL4 | PEL3 | PEL2 | PEL1 | PEL0 | | |
| SCRLAR | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | (33h) | Scroll area set |
| | 1 | ↑ | 1 | - | TFA15 | TFA14 | TFA13 | TFA12 | TFA11 | TFA10 | TFA9 | TFA8 | | Top fixed area (0,1,2, .., 319) |
| | 1 | ↑ | 1 | - | TFA7 | TFA6 | TFA5 | TFA4 | TFA3 | TFA2 | TFA1 | TFA0 | | |
| | 1 | ↑ | 1 | - | VSA15 | VSA14 | VSA13 | VSA12 | VSA11 | VSA10 | VSA9 | VSA8 | | Vertical scroll area (0,1,2, .., 319) |
| | 1 | ↑ | 1 | - | VSA7 | VSA6 | VSA5 | VSA4 | VSA3 | VSA2 | VSA1 | VSA0 | | |
| | 1 | ↑ | 1 | - | BFA15 | BFA14 | BFA13 | BFA12 | BFA11 | BFA10 | BFA9 | BFA8 | | Bottom fixed area (0,1,2, .., 319) |
| | 1 | ↑ | 1 | - | BFA7 | BFA6 | BFA5 | BFA4 | BFA3 | BFA2 | BFA1 | BFA0 | | |
| TEOFF | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | (34h) | Tearing effect line off |
| TEON | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | (35h) | Tearing effect mode set & on |
| | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TELOM | | M="0": Mode1, M="1": Mode2 |
| MADCTR | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | (36h) | Memory data access control |
| | 1 | ↑ | 1 | - | MY | MX | MV | ML | RGB | MH | 0 | 0 | | - |
| VSCSAD | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | (37h) | Scroll start address of RAM |
| | 1 | ↑ | 1 | - | SSA15 | SSA14 | SSA13 | SSA12 | SSA11 | SSA10 | SSA9 | SSA8 | | SSA = 0, 1, 2, …, 319 |
| | 1 | ↑ | 1 | - | SSA7 | SSA6 | SSA5 | SSA4 | SSA3 | SSA2 | SSA1 | SSA0 | | |
| IDMOFF | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | (38h) | Idle mode off |
| IDMON | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | (39h) | Idle mode on |
| COLMOD | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | (3Ah) | Interface pixel format |
| | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | IFPF2 | IFPF1 | IFPF0 | | Interface format |
| RDID1 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | (DAh) | Read ID1 |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | | Dummy read |
| | 1 | 1 | ↑ | - | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | | Read parameter |
| RDID2 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | (DBh) | Read ID2 |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | | Dummy read |
| | 1 | 1 | ↑ | - | ID27 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 | | Read parameter |
| RDID3 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | (DCh) | Read ID3 |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | | Dummy read |
| | 1 | 1 | ↑ | - | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 | | Read parameter |

"-": Don't care, can be set to VDDIO or VSS level

Table 6.1.1 System Function command List (4)

| Instruction | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Hex) | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WRDISBV | 0 | ↑ | 1 | - | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | (51h) | Write Display Brightness |
| | 1 | ↑ | 1 | - | DBV7 | DBV6 | DBV5 | DBV4 | DBV3 | DBV2 | DBV1 | DBV0 | | brightness value of the display. (0,1,2,..,255) |
| RDDISBV | 0 | ↑ | 1 | - | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | (52h) | Read Display Brightness Value |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - | Dummy read |
| | 1 | 1 | ↑ | - | DBV7 | DBV6 | DBV5 | DBV4 | DBV3 | DBV2 | DBV1 | DBV0 | | Read value of the display. |
| WRCTRLD | 0 | ↑ | 1 | - | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | (53h) | Write Control Display |
| | 1 | ↑ | 1 | - | - | - | BCTRL | - | DD | BL | - | - | - | |
| RDCTRLD | 0 | ↑ | 1 | | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | (54h) | Read CTRL Value Display |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - | Dummy read |
| | 1 | 1 | ↑ | - | 0 | 0 | BCTRL | 0 | DD | BL | 0 | 0 | | |
| WRCABC | 0 | ↑ | 1 | - | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | (55h) | Write Content Adaptive Brightness Control |
| | 1 | ↑ | 1 | - | - | - | - | - | - | - | C1 | C0 | | |
| RDCABC | 0 | ↑ | 1 | - | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | (56h) | Read Content Adaptive Brightness Control |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - | Dummy read |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | C1 | C0 | | |
| WRCABCMB | 0 | ↑ | 1 | - | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | (5Eh) | Write CABC minimum brightness |
| | 1 | ↑ | 1 | - | CMB7 | CMB6 | CMB5 | CMB4 | CMB3 | CMB2 | CMB1 | CMB0 | | |
| RDCABCMB | 0 | ↑ | 1 | - | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | (5Fh) | Read CABC minimum brightness |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - | Dummy read |
| | 1 | 1 | ↑ | - | CMB7 | CMB6 | CMB5 | CMB4 | CMB3 | CMB2 | CMB1 | CMB0 | | |
| RDABCSDR | 0 | ↑ | 1 | - | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | (68h) | Read Automatic Brightness Control Self-Diagnostic Result |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - | Dummy read |
| | 1 | 1 | ↑ | - | D7 | D6 | 0 | 0 | 0 | 0 | 0 | 0 | | |

"-": Don't care, can be set to VDDIO or VSS level

### 6.1.2. Panel Function Command List and Description

Table 6.1.2 list all the panel function command. Panel function command is only accessible when EXTC is pulled high state (by VDDIO).

Table 6.1.2 Panel Function command List (1)

| Instruction | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Hex) | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FRMCTR1 | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | (B1h) | In normal mode (Full colors)<br>FP0: Front porch in normal mode<br>BP0: Back porch in normal mode<br>RTN0: Number of clock / one line |
| | 1 | ↑ | 1 | - | - | - | - | - | FP [3] | FP [2] | FP [1] | FP [0] | | |
| | 1 | ↑ | 1 | - | - | - | - | - | BP [3] | BP [2] | BP [1] | BP [0] | | |
| | 1 | ↑ | 1 | - | - | - | RTN [5] | RTN [4] | RTN [3] | RTN [2] | RTN [1] | RTN [0] | | |
| INVCTR | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | (B4h) | Display inversion control<br>NLA, NLB, NLC: set inversion |
| | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | NLA | NLB | NLC | | |
| DISSET5 | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | (B6h) | Display function setting<br>NO: the amount of non-overlap<br>SDT: set amount of source delay<br>PT: No display area source/ VCOM/ Gate output control |
| | 1 | ↑ | 1 | - | 0 | 0 | NO1 | NO0 | SDT1 | STD0 | - | - | | |
| | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | PTG1 | PTG0 | PT1 | PT0 | | |
| FRADJ | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | (BAh) | Frame Rate ADJustment |
| | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | FR3 | FR2 | FR1 | FR0 | | |
| | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |

"-": Don't care, can be set to VDDIO or VSS level

Table 6.1.2 Panel Function Command List (2)

| Instruction | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Hex) | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWCTR1 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | (C0h) | Power control setting<br>VRH: Set the GVDD voltage<br>VC : Set the VCI1 voltage<br>Power control setting |
| | 1 | ↑ | 1 | - | 0 | 0 | 0 | VRH4 | VRH3 | VRH2 | VRH1 | VRH0 | | |
| | 1 | ↑ | 1 | | 0 | 0 | 0 | 0 | 0 | VC2 | VC1 | VC0 | | |
| PWCTR3 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | (C2h) | Set the amount of current in Operational amplifier |
| | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | AP2 | AP1 | AP0 | | |
| PWCTR4 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | (C3h) | BT:set AVDD/VCL/ VGH/ VGL voltage |
| | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | BT2 | BT1 | BT0 | | |
| PWCTR5 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | (C4h) | In partial mode + Full colors<br>DC: adjust the booster circuit for Idle mode |
| | 1 | ↑ | 1 | - | 0 | 0 | DC2 [1] | DC2 [0] | 0 | 0 | DC1 [1] | DC1 [0] | | |
| VMCTR1 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | (C5h) | VCOM control 1<br>nVM: VCOM input select<br>VMH: VCOMH voltage control |
| | 1 | ↑ | 1 | - | nVM | VMH6 | VMH 5 | VMH4 | VMH3 | VMH2 | VMH1 | VMH0 | | |
| VMCTR2 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | (C6h) | VCOM control 2<br>VMA: VCOMAC voltage control |
| | 1 | ↑ | 1 | - | 0 | VMA6 | VMA5 | VMA4 | VMA3 | VMA2 | VMA1 | VMA0 | | |
| RVMOF CTR | 0 | 1 | ↑ | - | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | (C8h) | VCOM control 4<br>Read the VMOF value form NV memory |
| | 1 | 1 | ↑ | - | nVM | RVMF 6 | RVMF 5 | RVMF 4 | RVMF 3 | RVMF 2 | RVMF 1 | RVMF 0 | | |
| PWCTR6 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | (CBh) | Set the amount of current in Operational amplifier |
| | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | GP2 | GP1 | GP0 | | |
| PWCTR7 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | (CCh) | Set the amount of current in Operational amplifier |
| | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | SP2 | SP1 | SP0 | | |

"-": Don't care, can be set to VDDIO or VSS level

Table 6.1.2 Panel Function Command List (3)

| Instruction | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Hex) | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WRID1 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | (D0h) | Panel version code<br>Write ID1 value to NV memory<br>Set the LCM version code at ID1 |
| | 1 | ↑ | 1 | - | 1 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | | |
| WRID2 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | (D1h) | Panel version code<br>Write ID2 value to NV memory<br>Set the LCM version code at ID2 |
| | 1 | ↑ | 1 | - | 1 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 | | |
| WRID3 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | (D2h) | Driver maker Project code<br>Write ID3 value to NV memory<br>Set the project code at ID3 |
| | 1 | ↑ | 1 | - | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 | | |
| RDID4 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | (D3h) | IC Vender Coder<br>Dummy read<br>ID41:IC Vender Coder<br>ID42: IC Part Number Coder<br>ID43 & ID44: Chip version coder |
| | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | | |
| | 1 | 1 | ↑ | - | ID417 | ID416 | ID415 | ID414 | ID413 | ID412 | ID411 | ID410 | | |
| | 1 | 1 | ↑ | - | ID427 | ID426 | ID425 | ID424 | ID423 | ID422 | ID421 | ID420 | | |
| | 1 | 1 | ↑ | - | ID437 | ID436 | ID435 | ID434 | ID43 | ID432 | ID431 | ID430 | | |
| | 1 | 1 | ↑ | - | ID447 | ID446 | ID445 | ID444 | ID443 | ID442 | ID441 | ID440 | | |
| NVCTR1 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | (D9h) | NV memory function controller 1<br>Please refer to 'OTP programming procedure' for details. |
| NVCTR2 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | (DEh) | NV memory function controller 2<br>Please refer to 'OTP programming procedure' for details. |
| | 1 | 1 | ↑ | - | 0 | SMY | SMX | SRGB | 0 | 0 | LCM1 | LCM0 | | |
| NVCTR3 | 0 | ↑ | 1 | | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | (DFh) | NV memory function controller 3<br>Please refer to 'OTP programming procedure' for details. |
| | 1 | ↑ | 1 | - | - | VMH6 | VMH5 | VMH4 | VMH3 | VMH2 | VMH1 | VMH0 | | |
| | 1 | ↑ | 1 | - | - | VMA6 | VMA5 | VMA4 | VMA3 | VMA2 | VMA1 | VMA0 | | |

"-": Don't care, can be set to VDDIO or VSS level

Table 6.1.2 Panel Function Command List (4)

| Instruction | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Hex) | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GAMCTRP | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | (E0h) | Gamma adjustment |
| | 1 | ↑ | 1 | - | - | - | PVR1V0[5] | PVR1V0[4] | PVR1V0[3] | PVR1V0[2] | PVR1V0[1] | PVR1V0[0] | | |
| | 1 | ↑ | 1 | - | - | - | PVR1V1[5] | PVR1V1[4] | PVR1V1[3] | PVR1V1[2] | PVR1V1[1] | PVR1V1[0] | | |
| | 1 | ↑ | 1 | - | - | - | PVR1V2[5] | PVR1V2[4] | PVR1V2[3] | PVR1V2[2] | PVR1V2[1] | PVR1V2[0] | | |
| | 1 | ↑ | 1 | - | - | - | PVR1V61[5] | PVR1V61[4] | PVR1V61[3] | PVR1V61[2] | PVR1V61[1] | PVR1V61[0] | | |
| | 1 | ↑ | 1 | - | - | - | PVR1V62[5] | PVR1V62[4] | PVR1V62[3] | PVR1V62[2] | PVR1V62[1] | PVR1V62[0] | | |
| | 1 | ↑ | 1 | - | - | - | PVR1V63[5] | PVR1V63[4] | PVR1V63[3] | PVR1V63[2] | PVR1V63[1] | PVR1V63[0] | | |
| | 1 | ↑ | 1 | - | - | - | PVR2V13[5] | PVR2V13[4] | PVR2V13[3] | PVR2V13[2] | PVR2V13[1] | PVR2V13[0] | | |
| | 1 | ↑ | 1 | - | - | - | PVR2V50[5] | PVR2V50[4] | PVR2V50[3] | PVR2V50[2] | PVR2V50[1] | PVR2V50[0] | | |
| | 1 | ↑ | 1 | - | - | - | - | - | PVR3V4[3] | PVR3V4[2] | PVR3V4[1] | PVR3V4[0] | | |
| | 1 | ↑ | 1 | - | - | - | - | - | PVR3V8[3] | PVR3V8[2] | PVR3V8[1] | PVR3V8[0] | | |
| | 1 | ↑ | 1 | - | - | - | - | - | PVR3V20[3] | PVR3V20[2] | PVR3V20[1] | PVR3V20[0] | | |
| | 1 | ↑ | 1 | - | - | - | - | - | PVR3V27[3] | PVR3V27[2] | PVR3V27[1] | PVR3V27[0] | | |
| | 1 | ↑ | 1 | - | - | - | - | - | PVR3V36[3] | PVR3V36[2] | PVR3V36[1] | PVR3V36[0] | | |
| | 1 | ↑ | 1 | - | - | - | - | - | PVR3V43[3] | PVR3V43[2] | PVR3V43[1] | PVR3V43[0] | | |

"-": Don't care, can be set to VDDIO or VSS level

Table 6.1.2 Panel Function Command List (5)

| Instruction | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Hex) | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GAMCTRN | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | (E1h) | Gamma adjustment |
| | 1 | ↑ | 1 | - | - | - | NVR1V0[5] | NVR1V0[4] | NVR1V0[3] | NVR1V0[2] | NVR1V0[1] | NVR1V0[0] | | |
| | 1 | ↑ | 1 | - | - | - | NVR1V1[5] | NVR1V1[4] | NVR1V1[3] | NVR1V1[2] | NVR1V1[1] | NVR1V1[0] | | |
| | 1 | ↑ | 1 | - | - | - | NVR1V2[5] | NVR1V2[4] | NVR1V2[3] | NVR1V2[2] | NVR1V2[1] | NVR1V2[0] | | |
| | 1 | ↑ | 1 | - | - | - | NVR1V61[5] | NVR1V61[4] | NVR1V61[3] | NVR1V61[2] | NVR1V61[1] | NVR1V61[0] | | |
| | 1 | ↑ | 1 | - | - | - | NVR1V62[5] | NVR1V62[4] | NVR1V62[3] | NVR1V62[2] | NVR1V62[1] | NVR1V62[0] | | |
| | 1 | ↑ | 1 | - | - | - | NVR1V63[5] | NVR1V63[4] | NVR1V63[3] | NVR1V63[2] | NVR1V63[1] | NVR1V63[0] | | |
| | 1 | ↑ | 1 | - | - | - | NVR2V13[5] | NVR2V13[4] | NVR2V13[3] | NVR2V13[2] | NVR2V13[1] | NVR2V13[0] | | |
| | 1 | ↑ | 1 | - | - | - | NVR2V50[5] | NVR2V50[4] | NVR2V50[3] | NVR2V50[2] | NVR2V50[1] | NVR2V50[0] | | |
| | 1 | ↑ | 1 | - | - | - | - | - | NVR3V4[3] | NVR3V4[2] | NVR3V4[1] | NVR3V4[0] | | |
| | 1 | ↑ | 1 | - | - | - | - | - | NVR3V8[3] | NVR3V8[2] | NVR3V8[1] | NVR3V8[0] | | |
| | 1 | ↑ | 1 | - | - | - | - | - | NVR3V20[3] | NVR3V20[2] | NVR3V20[1] | NVR3V20[0] | | |
| | 1 | ↑ | 1 | - | - | - | - | - | NVR3V27[3] | NVR3V27[2] | NVR3V27[1] | NVR3V27[0] | | |
| | 1 | ↑ | 1 | - | - | - | - | - | NVR3V36[3] | NVR3V36[2] | NVR3V36[1] | NVR3V36[0] | | |
| | 1 | ↑ | 1 | - | - | - | - | - | NVR3V43[3] | NVR3V43[2] | NVR3V43[1] | NVR3V43[0] | | |

"-": Don't care, can be set to VDDIO or VSS level

### 6.2. System Command Description

#### 6.2.1. NOP (00h)

| 00H | NOP (No Operation) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| NOP | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | (00h) |
| Parameter | No Parameter | | | | | | | | | | | | - |

NOTE: "-" Don't care, can be set to VDDIO or VSS level, can be set to VDDIO or VSS level

| | |
|---|---|
| Description | -This command is empty command. It does not have effect on the display module.<br>-However it can be used to terminate RAM data write or read as described in RAMWR (Memory Write), RAMHD (Memory Read) and parameter write commands. |
| Restriction | - |
| Register Availability | Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes<br>Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes<br>Status: Sleep In — Availability: Yes |
| Default | Status: Power On Sequence — Default Value: N/A<br>Status: S/W Reset — Default Value: N/A<br>Status: H/W Reset — Default Value: N/A |
| Flow Chart | - |

#### 6.2.2. SWRESET (01h): Software Reset

| 01H | SWRESET (Software Reset) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| SWRESET | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | (01h) |
| Parameter | No Parameter | | | | | | | | | | | | - |

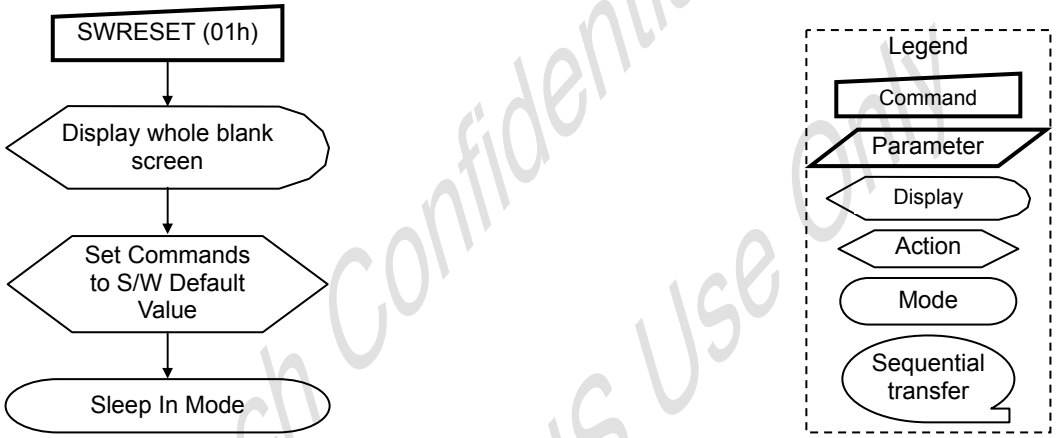
*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

| | |
|---|---|
| Description | -When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values and all source outputs are set to VSS (display off). (See default tables in each command description)<br>*Note: The Frame Memory contents are not affected by this command.* |
| Restriction | -It will be necessary to wait 5msec before sending new command following software reset.<br>-The display module loads all display supplier's factory default values to the registers during 5msec.<br>-If Software Reset is applied during Sleep Out mode, it will be necessary to wait *120msec* before sending Sleep Out command.<br>-Software Reset command cannot be sent during Sleep Out sequence. |
| Register Availability | Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes<br>Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes<br>Status: Sleep In — Availability: Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | N/A |
| S/W Reset | N/A |
| H/W Reset | N/A |

Flow Chart



### 6.2.3. RDDID (04h): Read Display ID

| 04H | RDDID (Read Display ID) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| RDDID | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | (04h) |
| 1st Parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd Parameter | 1 | 1 | ↑ | - | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | |
| 3rd Parameter | 1 | 1 | ↑ | - | ID27 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 | |
| 4th Parameter | 1 | 1 | ↑ | - | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-This read byte returns 24-bits display identification information.

-The 1st parameter is dummy data

-The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.

-The 3rd parameter (ID27 to ID20): LCD module/driver version ID

-The 4th parameter (ID37 to UD30): LCD module/driver ID.

*NOTE: Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.*

**Restriction**

-

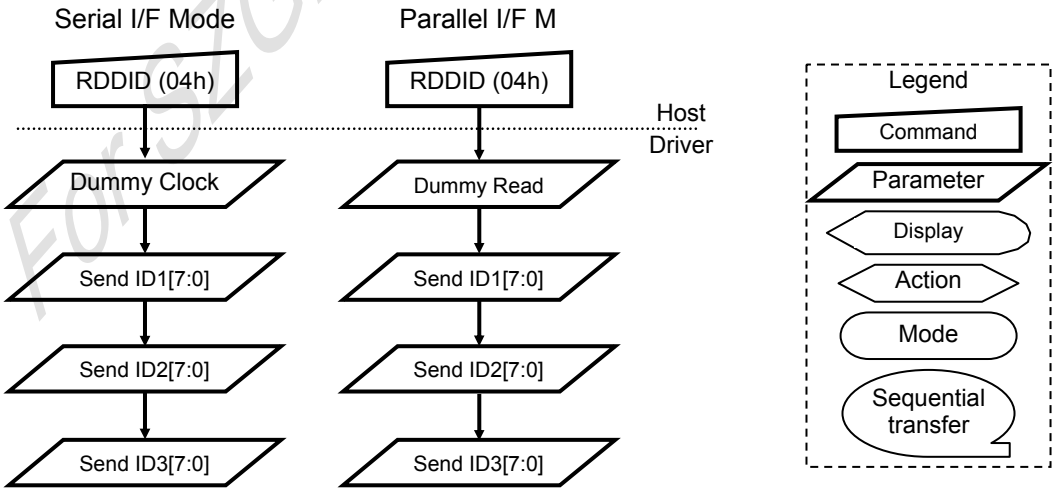
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | | |
|---|---|---|---|
| | ID1 | ID2 | ID3 |
| Power On Sequence | 38h | 8xh | 4Fh |
| S/W Reset | 38h | 8xh | 4Fh |
| H/W Reset | 38h | 8xh | 4Fh |

**Flow Chart**



### 6.2.4. RDDST (09h): Read Display Status

| 09H | RDDST (Read Display Status) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| RDDST | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | (09h) |
| 1st Parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd Parameter | 1 | 1 | ↑ | - | BSTON | MY | MX | MV | ML | RGB | MH | ST24 | |
| 3rd Parameter | 1 | 1 | ↑ | - | ST23 | IFPF2 | IFPF1 | IFPF0 | IDMON | PTLON | SLOUT | NORON | |
| 4th Parameter | 1 | 1 | ↑ | - | VSSON | ST14 | INVON | ST12 | ST11 | DISON | TEON | GCS2 | |
| 5th Parameter | 1 | 1 | ↑ | | GCS1 | GCS0 | TELOM | ST4 | ST3 | ST2 | ST1 | ST0 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

Description

This command indicates the current status of the display as described in the table below:

| Bit | Description | Value |
|---|---|---|
| BSTON | Booster Voltage Status | '1' =Booster on,<br>'0' =Booster off |
| MY | Row Address Order (MY) | '1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1')<br>'0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0') |
| MX | Column Address Order (MX) | '1' =Decrement, (Right to Left, when MADCTL (36h) D6='1')<br>'0' =Increment, (Left to Right, when MADCTL (36h) D6='0') |
| MV | Row/Column Exchange (MV) | '1' = Row/column exchange, (when MADCTL (36h) D5='1')<br>'0' = Normal, (when MADCTL (36h) D5='0') |
| ML | Vertical Refresh Order (ML) | '1' =Decrement, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1')<br>"0"=Increment, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0') |
| RGB | RGB/ BGR Order (RGB) | '1' =BGR, (When MADCTL (36h) D3='1')<br>'0' =RGB, (When MADCTL (36h) D3='0') |
| MH | Horizontal Order (MH) | '1' =Decrement, (LCD refresh Right to Left, when MADCTL (36h) D2='1')<br>'0' =Increment, (LCD refresh Left to Right, when MADCTL (36h) D2='0') |
| ST24 | For Future Use | '0' |
| ST23 | For Future Use | '0' |
| IFPF2<br>IFPF1<br>IFCPF0 | Interface Color Pixel Format Definition | "011" = 12-bits / pixel,<br>"101" = 16-bits / pixel,<br>"110" = 18-bits / pixel,others are no define |
| IDMON | Idle Mode On/Off | '1' = On, "0" = Off |
| PTLON | Partial Mode On/Off | '1' = On, "0" = Off |
| SLPOUT | Sleep In/Out | '1' = Out, "0" = In |
| NORON | Display Normal Mode On/Off | '1' = Normal Display,<br>'0' = Partial Display |
| VSSON | Vertical Scrolling Status | '1' = Scroll on,"0" = Scroll off |
| ST14 | Horizontal Scroll Status | '0' |
| INVON | Inversion Status | '1' = On, "0" = Off |
| ST12 | All Pixels On (Not Used) | '0' |
| ST11 | All Pixels Off (Not Used) | '0' |
| DISON | Display On/Off | '1' = On, "0" = Off |
| TEON | Tearing effect line on/off | '1' = On, "0" = Off |
| GCSEL2<br>GCSEL1<br>GCSEL0 | Gamma Curve Selection | "000" = GC0<br>"001" = GC1<br>"010" = GC2<br>"011" = GC3<br>"100" to "111" = Not defined |
| TELOM | Tearing effect line mode | '0' = mode1, '1' = mode2 |
| ST4 | Horizontal Sync. (Not Used) | '0' |
| ST3 | Vertical Sync, (Not Used) | '0' |
| ST2 | Pixel Clock(Not Used) | '0' |
| ST1 | Data Enable(Not Used) | '0' |
| ST0 | For Future Use | '0' |

*Note: ST0, ST11-ST12, ST14, ST23, ST24 are set to '0'*

| | |
|---|---|
| Restriction | - |

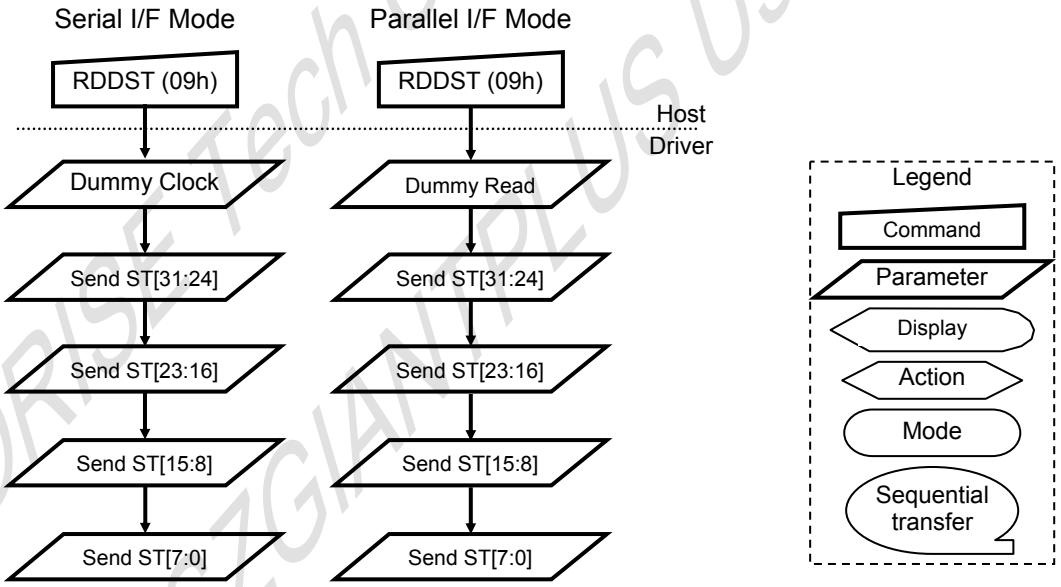
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value (ST31 to ST0) | | | |
|---|---|---|---|---|
| | ST[31-24] | ST[23-16] | ST[15-8] | ST[7-0] |
| Power On Sequence | 0000-0000 | 0110-0001 | 0000-0000 | 0000-0000 |
| S/W Reset | 0xxx-xx00 | 0xxx-0001 | 0000-0000 | 0000-0000 |
| H/W Reset | 0000-0000 | 0110-0001 | 0000-0000 | 0000-0000 |

**Flow Chart**



### 6.2.5. RDDPM (0Ah): Read Display Power Mode

| 0AH | RDDPM (Read Display Power Mode) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| RDDPM | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | (0Ah) |
| 1st Parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd Parameter | 1 | 1 | ↑ | | BSTON | IDMON | PTLON | SLPOUT | NORON | DISON | D1 | D0 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

This command indicates the current status of the display as described in the table below:

| Bit | Description | Value |
|---|---|---|
| BSTON | Booster Voltage Status | "1"=Booster on,<br>"0"=Booster off |
| IDMON | Idle Mode On/Off | "1" = Idle Mode On,<br>"0" = Idle Mode Off |
| PTLON | Partial Mode On/Off | "1" = Partial Mode On,<br>"0" = Partial Mode Off |
| SLPON | Sleep In/Out | "1" = Sleep Out,<br>"0" = Sleep In |
| NORON | Display Normal Mode On/Off | "1" = Normal Display,<br>"0" = Partial Display |
| DISON | Display On/Off | "1" = Display On,<br>"0" = Display Off |
| D1 | Not Used | "0" |
| D0 | Not Used | "0" |

**Restriction**

-

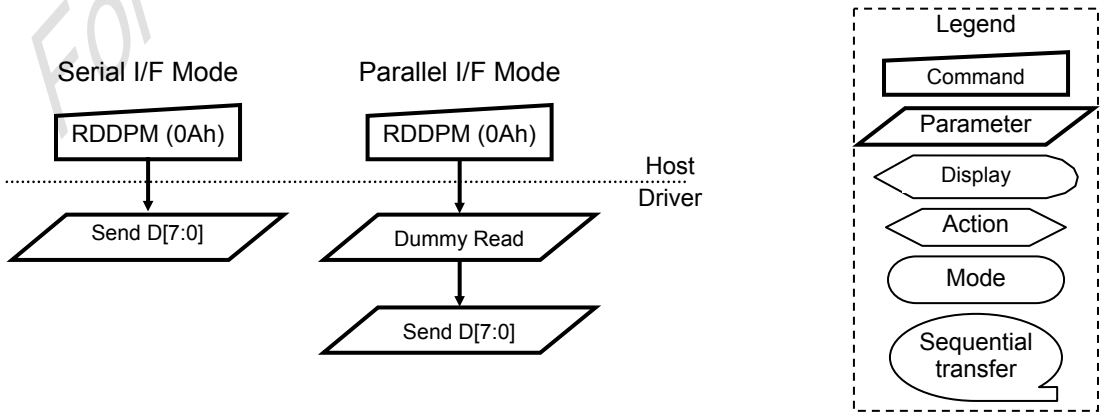
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value (D7 to D0) |
|---|---|
| Power On Sequence | 0000_1000 (08h) |
| S/W Reset | 0000_1000 (08h) |
| H/W Reset | 0000_1000 (08h) |

**Flow Chart**



### 6.2.6. RDDMADCTR (0Bh): Read Display MADCTR

| 0BH | RDDMADCTR (Read Display MADCTR) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| RDDMADCTR | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | (0Bh) |
| 1st Parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd Parameter | 1 | 1 | ↑ | | MX | MY | MV | ML | RGB | MH | D1 | D0 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

This command indicates the current status of the display as described in the table below:

| Bit | Description | Value |
|---|---|---|
| MX | Row Address Order | '1' = Bottom to Top (When MADCTL B7='1')<br>'0' = Top to Bottom (When MADCTL B7='0') |
| MY | Column Address Order | '1' = Right to Left (When MADCTL B6='1')<br>'0' = Left to Right (When MADCTL B6='0') |
| MV | Row/Column Order (MV) | '1' = Row/column exchange (MV=1)<br>'0' = Normal (MV=0) |
| ML | Vertical Refresh Order | '1' =LCD Refresh Bottom to Top<br>'0' =LCD Refresh Top to Bottom |
| RGB | RGB/BGR Order | '1' =BGR, "0"=RGB |
| MH | Horizontal order | '1' =LCD Refresh Right to Left<br>'0' =LCD Refresh Left to Right |
| D1 | Not Used | '0' |
| D0 | Not Used | '0' |

**Restriction**

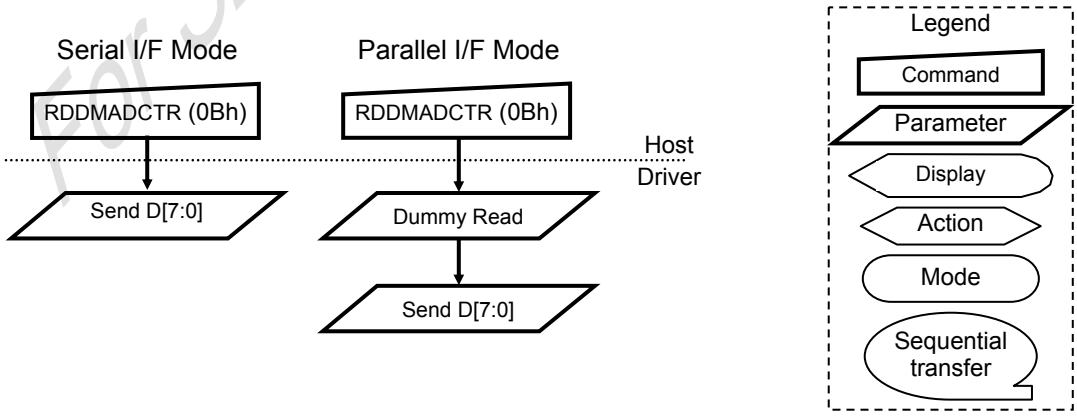
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value (D7 to D0) |
|---|---|
| Power On Sequence | 0000_0000 (00h) |
| S/W Reset | No change |
| H/W Reset | 0000_0000 (00h) |

**Flow Chart**



### 6.2.7. RDDCOLMOD (0Ch): Read Display Pixel Format

| 0CH | RDDCOLMOD (Read Display Pixel Format) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| RDDCOLMOD | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | (0Ch) |
| 1st Parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd Parameter | 1 | 1 | ↑ | - | - | - | - | - | - | IFPF2 | IFPF1 | IFPF0 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-This command indicates the current status of the display as described in the table below:

| IFPF[2:0] | | MCU Interface Color Format |
|---|---|---|
| 011 | 3 | 12-bits/pixel |
| 101 | 5 | 16-bits/pixel |
| 110 | 6 | 18-bits/pixel |
| 111 | 7 | No used |

Others are no define and invalid

**Restriction**

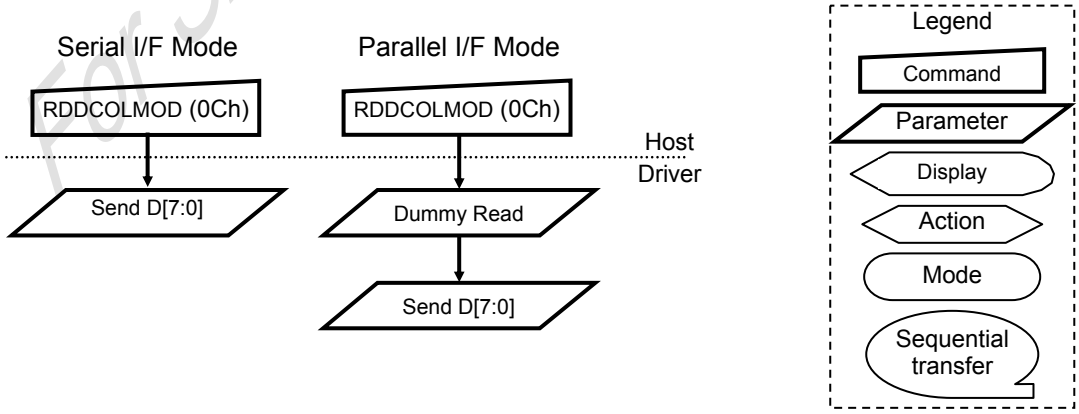
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| | IFPF[2:0] |
| Power On Sequence | 0110 (18-bits/pixel) |
| S/W Reset | No Change |
| H/W Reset | 0110 (18-bits/pixel) |

**Flow Chart**



### 6.2.8. RDDIM (0Dh): Read Display Image Mode

| 0DH | RDDIM (0Dh): Read Display Image Mode | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| RDDIM | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | (0Dh) |
| 1st Parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd Parameter | 1 | 1 | ↑ | - | VSSON | D6 | INVON | D4 | D3 | GCS2 | GCS1 | GCS0 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

This command indicates the current status of the display as described in the table below:

| Bit | Description | Value |
|---|---|---|
| VSSON | Vertical Scrolling On/Off | "1" = Vertical scrolling is On,<br>"0" = Vertical scrolling is Off |
| D6 | Horizontal Scrolling On/Off | "0" (Not used) |
| INVON | Inversion On/Off | "1" = Inversion is On,<br>"0" = Inversion is Off |
| D4 | All Pixels On | "0" (Not used) |
| D3 | All Pixels Off | "0" (Not used) |
| GCS2 | Gamma Curve Selection | "000" = GC0,<br>"001" = GC1,<br>"010" = GC2,<br>"011" = GC3, "100" to "111" = Not defined |
| GCS1 | | |
| GCS0 | | |

**Restriction**

-

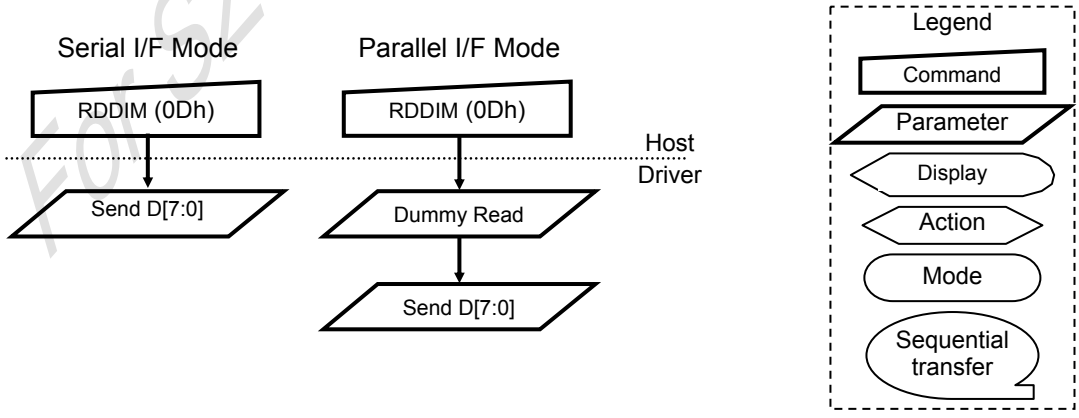
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value (D7 to D0) |
|---|---|
| Power On Sequence | 0000_0000 (00h) |
| S/W Reset | 0000_0000 (00h) |
| H/W Reset | 0000_0000 (00h) |

**Flow Chart**



### 6.2.9. RDDSM (0Eh): Read Display Signal Mode

| 0EH | RDDSM (0Eh): Read Display Signal Mode | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| RDDSM | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | (0Eh) |
| 1st Parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd Parameter | 1 | 1 | ↑ | - | TEON | TELOM | D5 | D4 | D3 | D2 | D1 | D0 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

This command indicates the current status of the display as described in the table below:

| Bit | Description | Value |
|---|---|---|
| TEON | Tearing Effect Line On/Off | "1" = On,<br>"0" = Off |
| TELOM | Tearing effect line mode | "0" = mode1,<br>"1" = mode2 |
| D5 | Not Used | "1" = On,<br>"0" = Off |
| D4 | Not Used | "1" = On,<br>"0" = Off |
| D3 | Not Used | "1" = On,<br>"0" = Off |
| D2 | Not Used | "1" = On,<br>"0" = Off |
| D1 | Not Used | "1" = On,<br>"0" = Off |
| D0 | Not Used | "1" = On,<br>"0" = Off |

**Restriction**

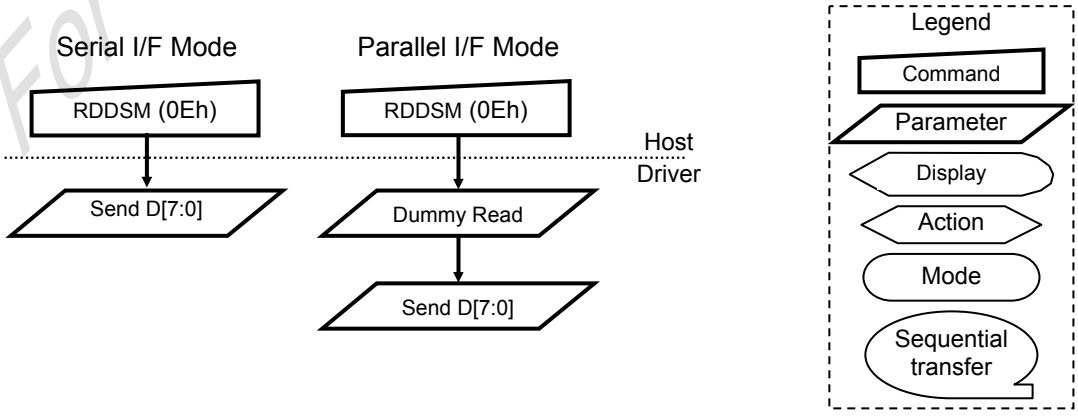
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value (D7 to D0) |
|---|---|
| Power On Sequence | 0000_0000 (00h) |
| S/W Reset | 0000_0000 (00h) |
| H/W Reset | 0000_0000 (00h) |

**Flow Chart**



### 6.2.10. RDDSDR (0Fh): Read Display Self-Diagnostic Result

| 0FH | RDDSDR (0Fh): Read Display Self-Diagnostic Result | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| RDDSDR | 0 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | (0Fh) |
| 1st Parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd Parameter | 1 | 1 | ↑ | - | RELD | FUND | D5 | D4 | D3 | D2 | D1 | D0 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

This command indicates the current status of the display as described in the table below:

| Bit | Description | Value |
|---|---|---|
| RELD | Register Loading Detection | |
| FUND | Functionality Detection | |
| D5 | Not Used | "1" |
| D4 | Not Used | "0" |
| D3 | Not Used | "0" |
| D2 | Not Used | "0" |
| D1 | Not Used | "0" |
| D0 | Not Used | "0" |

**Restriction**

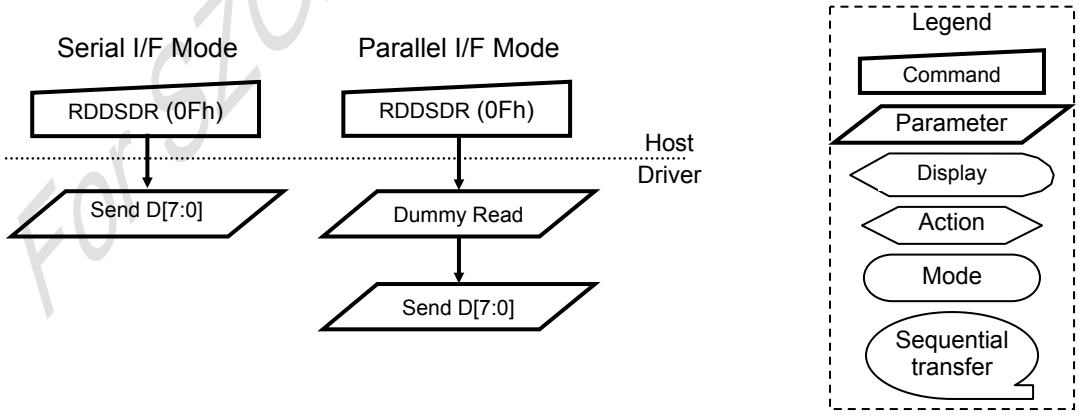
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value (D7 to D0) |
|---|---|
| Power On Sequence | 0000_0000 (00h) |
| S/W Reset | 0000_0000 (00h) |
| H/W Reset | 0000_0000 (00h) |

**Flow Chart**



### 6.2.11. SLPIN (10h): Sleep In

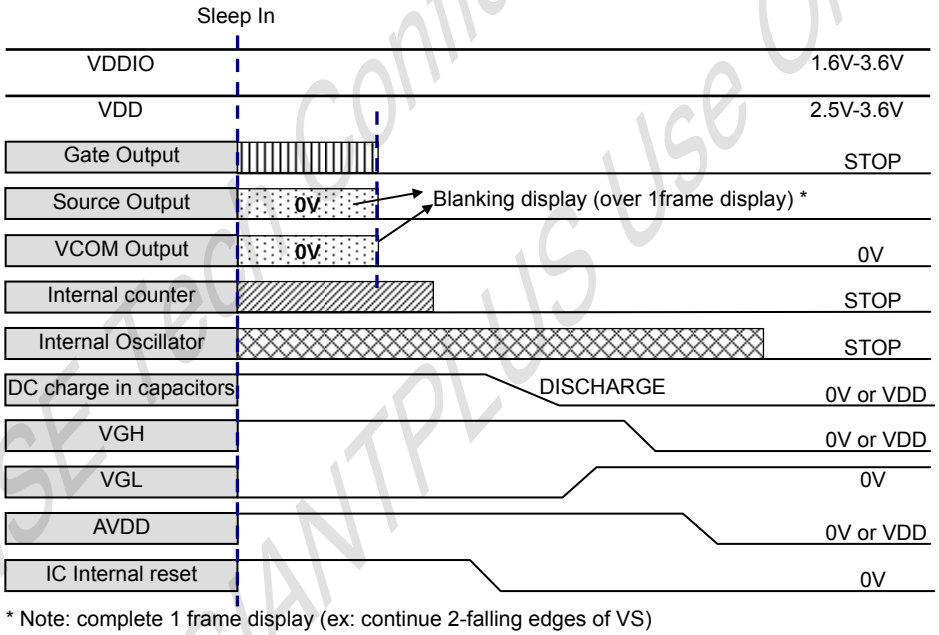
| 10H | SLPIN (Sleep In) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| SLPIN | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | (10h) |
| 1st Parameter | No parameter | | | | | | | | | | | | - |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-This command causes the LCD module to enter the minimum power consumption mode.

-In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.




* Note: complete 1 frame display (ex: continue 2-falling edges of VS)

-MCU interface and memory are still working and the memory keeps its contents

**Restriction**

-This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).

-It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.

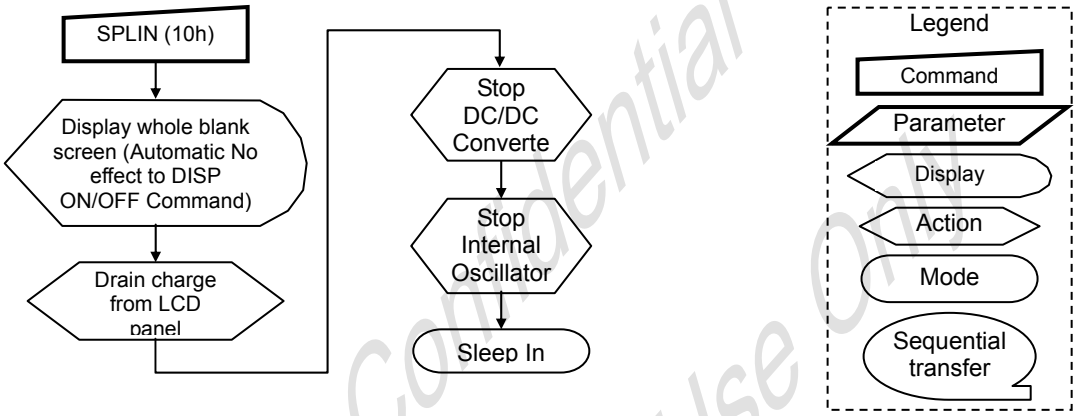
-It will be necessary to wait *120msec* after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Sleep in mode |
| S/W Reset | Sleep in mode |
| H/W Reset | Sleep in mode |

| | |
|---|---|
| Flow Chart | -It takes about 120msec to get into Sleep In mode (booster off state) after SLPIN command issued.<br>-The results of booster off can be check by RDDST (09h) command Bit31.<br>  |

### 6.2.12. SLPOUT (11h): Sleep Out

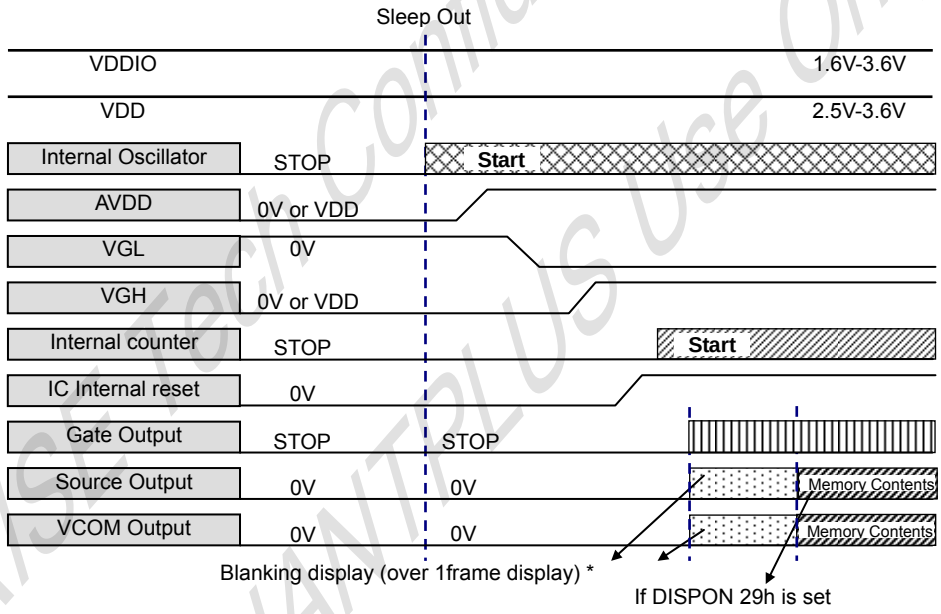
| 11H | SLPOUT (Sleep Out) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| SLPOUT | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | (11h) |
| 1st Parameter | No Parameter | | | | | | | | | | | | - |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-This command turns off sleep mode.

-In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.




* Note: complete 1 frame display (ex: continue 2-falling edges of VS)

**Restriction**

-This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h).

-It will be necessary to wait *5msec* before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.

-DRIVER loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the DRIVER is already Sleep Out mode.

-DRIVER is doing self-diagnostic functions during this *5msec*.

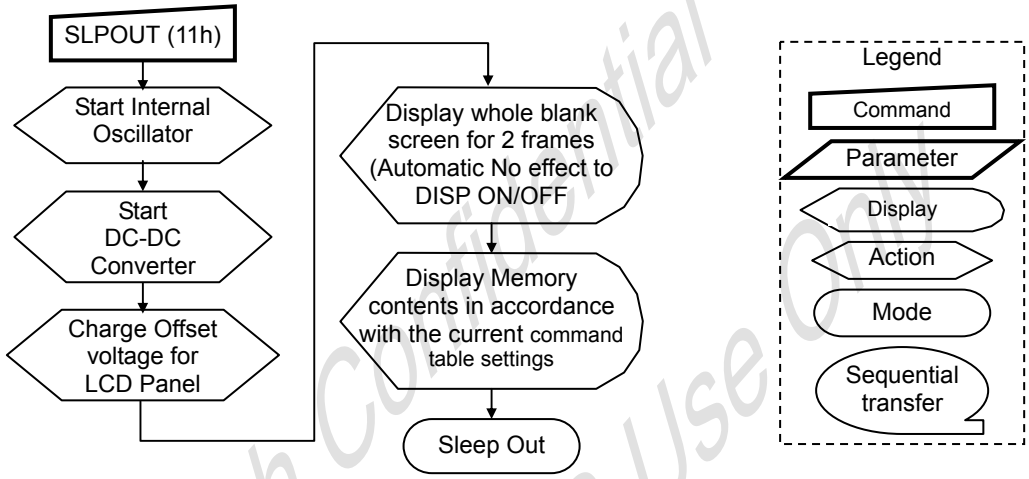
-It will be necessary to wait *120msec* after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Sleep in mode |
| S/W Reset | Sleep in mode |
| H/W Reset | Sleep in mode |

| | |
|---|---|
| Flow Chart | -It takes 120msec to become Sleep Out mode (booster on mode) after SLPOUT command issued.<br>-The results of booster on can be checked by RDDST (09h) command Bit31.<br>  |

### 6.2.13. PTLON (12h): Partial Display Mode On

| 12H | PTLON (12h): Partial Display Mode On | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| PTLON | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | (12h) |
| 1st Parameter | No Parameter | | | | | | | | | | | | - |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

| | |
|---|---|
| Description | -This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h)<br>-To leave Partial mode, the Normal Display Mode On command (13H) should be written.<br>-There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On. |
| Restriction | This command has no effect when Partial mode is active. |
| Register Availability | Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes<br>Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes<br>Status: Sleep In — Availability: Yes |
| Default | Status: Power On Sequence — Default Value: Normal Mode On<br>Status: S/W Reset — Default Value: Normal Mode On<br>Status: H/W Reset — Default Value: Normal Mode On |
| Flow Chart | See Partial Area (30h) |

### 6.2.14. NORON (13h): Normal Display Mode On

| 13H | NORON (Normal Display Mode On) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| NORON | 0 | ↑ | 1 | - | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | (13h) |
| 1st Parameter | No Parameter | | | | | | | | | | | | - |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

| | |
|---|---|
| Description | -This command returns the display to normal mode.<br>-Normal display mode on means Partial mode off, Scroll mode Off.<br>-Exit from NORON by the Partial mode On command (12h)<br>-There is no abnormal visual effect during mode change from Normal mode On to Partial mode On. |
| Restriction | -This command has no effect when Normal Display mode is active. |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out: Yes<br>Normal Mode On, Idle Mode On, Sleep Out: Yes<br>Partial Mode On, Idle Mode Off, Sleep Out: Yes<br>Partial Mode On, Idle Mode On, Sleep Out: Yes<br>Sleep In: Yes |
| Default | Status / Default Value<br>Power On Sequence: Normal Mode On<br>S/W Reset: Normal Mode On<br>H/W Reset: Normal Mode On |
| Flow Chart | -See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command |

### 6.2.15. INVOFF (20h): Display Inversion Off

| 20H | INVOFF (Display Inversion Off) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| INVOFF | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | (20h) |
| 1st Parameter | No Parameter | | | | | | | | | | | | - |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

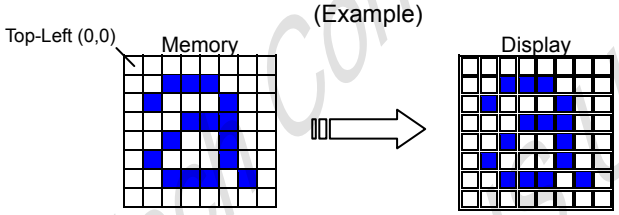
**Description**

-This command is used to recover from display inversion mode.

-This command makes no change of contents of frame memory.

-This command does not change any other status.

(Example)




**Restriction**

-This command has no effect when module is already inversion off mode.

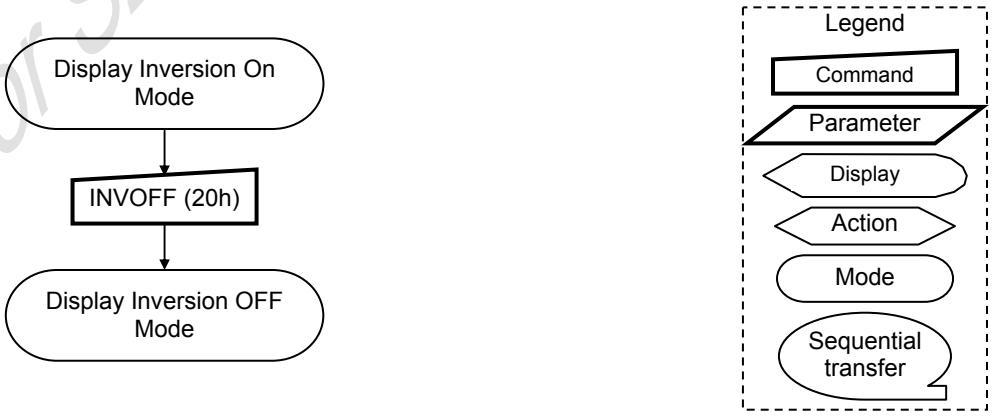
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Display Inversion off |
| S/W Reset | Display Inversion off |
| H/W Reset | Display Inversion off |

**Flow Chart**



### 6.2.16. INVON (21h): Display Inversion On

| 21H | INVON (Display Inversion On) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| INVON | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | (21h) |
| 1st Parameter | No Parameter | | | | | | | | | | | | - |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

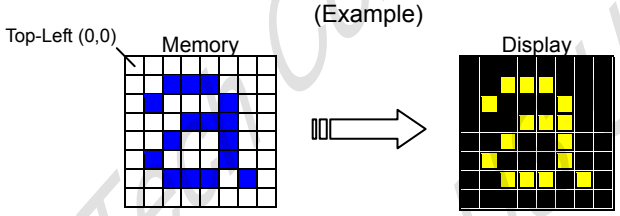
-This command is used to enter into display inversion mode

-This command makes no change of contents of frame memory.

-This command does not change any other status.

-To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.

(Example)




**Restriction**

-This command has no effect when module is already Inversion On mode.

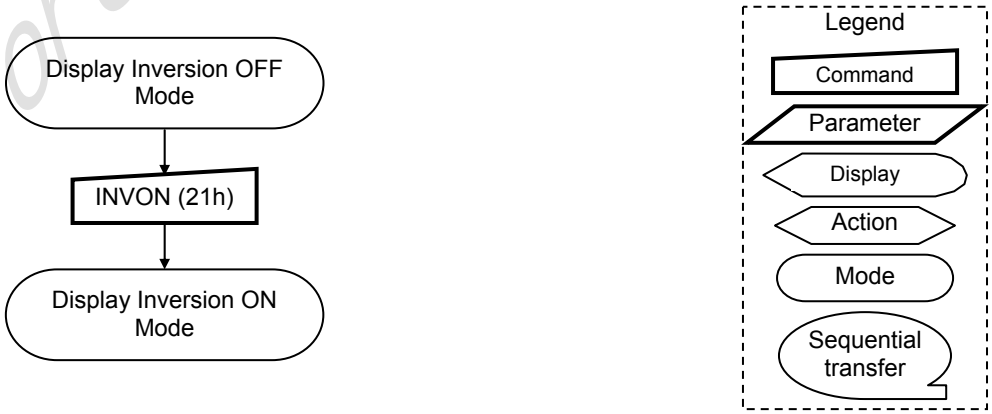
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Display Inversion off |
| S/W Reset | Display Inversion off |
| H/W Reset | Display Inversion off |

**Flow Chart**



### 6.2.17. GAMSET (26h): Gamma Set

| 26H | GAMSET (Gamma Set) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| GAMSET | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | (26h) |
| 1st Parameter | 1 | ↑ | 1 | - | GC7 | GC6 | GC5 | GC4 | GC3 | GC2 | GC1 | GC0 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.

| GC [7:0] | Parameter | Curve Selected |
|---|---|---|
| 01h | GC0 | Gamma Curve 1 (G2.2) |
| 02h | GC1 | Gamma Curve 2 (G1.8) |
| 04h | GC2 | Gamma Curve 3 (G2.5) |
| 08h | GC3 | Gamma Curve 4 (G1.0) |

*Note: All other values are undefined.*

**Restriction**

-Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid is received.

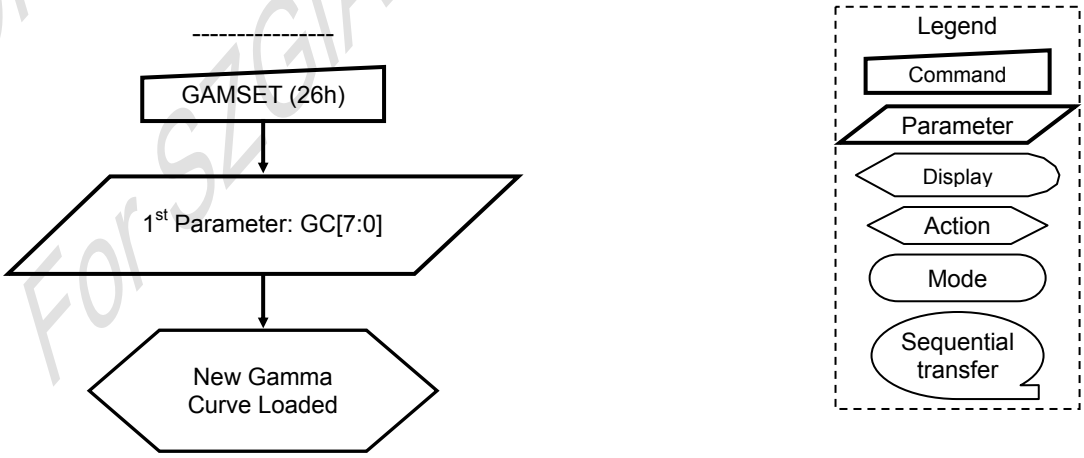
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 01h |
| S/W Reset | 01h |
| H/W Reset | 01h |

**Flow Chart**



### 6.2.18. DISPOFF (28h): Display Off

| 28H | DISPOFF (Display Off) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| DISPOFF | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | (28h) |
| 1st Parameter | No Parameter | | | | | | | | | | | | - |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disables and blank page inserted.

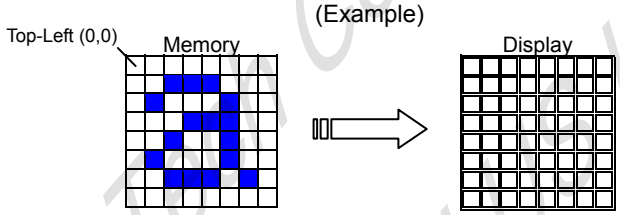
-This command makes no change of contents of frame memory.

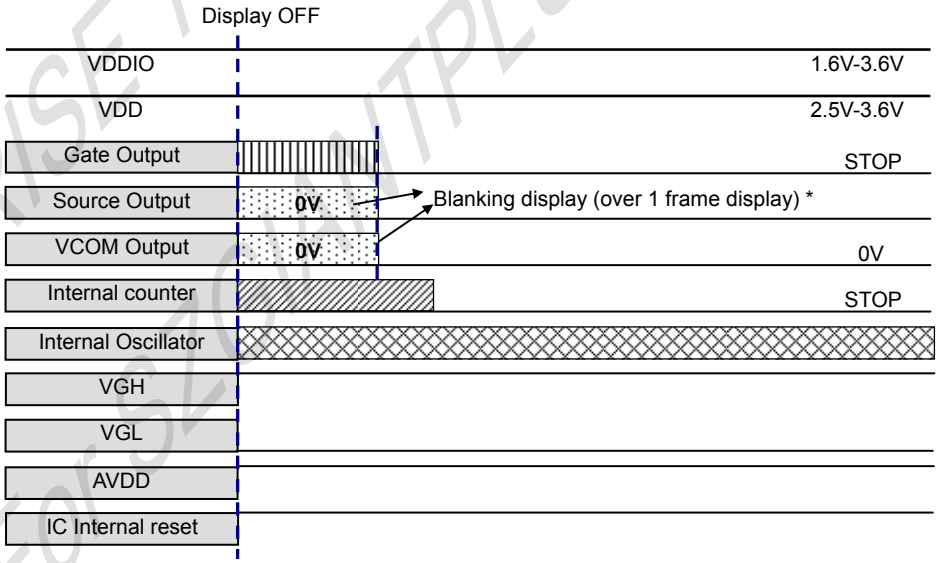
-This command does not change any other status.

-There will be no abnormal visible effect on the display.

-Exit from this command by Display On (29h)

(Example)




* Note: complete 1 frame display (ex: continue 2-falling edges of VS)

**Restriction**

-This command has no effect when module is already in Display Off mode.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | Display off |
| S/W Reset | Display off |
| H/W Reset | Display off |

Flow Chart

### 6.2.19. DISPON (29h): Display On

| 29H | DISPON (Display On) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| DISPON | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | (29h) |
| 1st Parameter | No Parameter | | | | | | | | | | | | - |

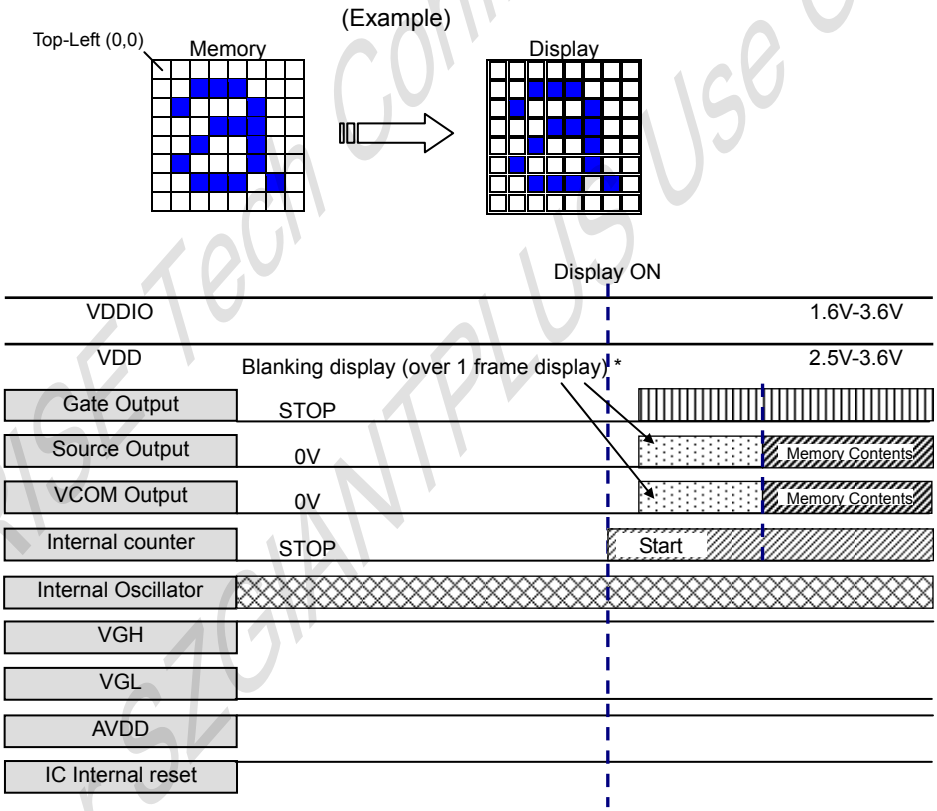
*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.

-This command makes no change of contents of frame memory.

-This command does not change any other status.




* Note: complete 1 frame display (ex: continue 2-falling edges of VS)

**Restriction**

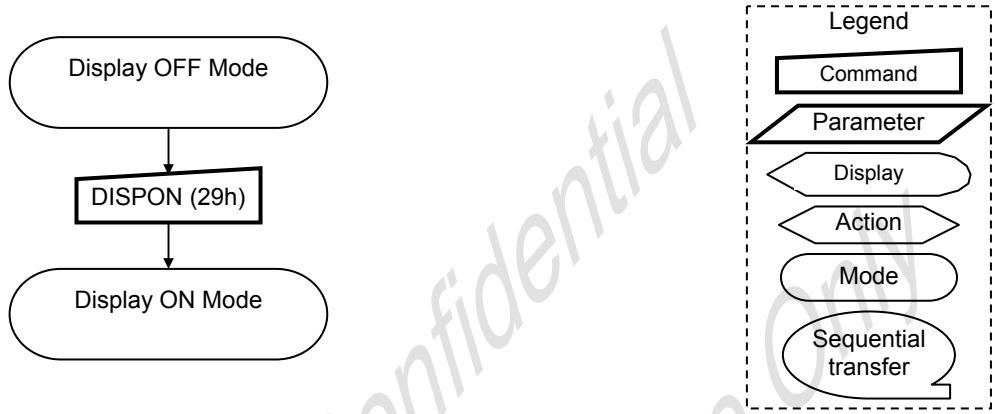
-This command has no effect when module is already in Display On mode.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Display off |
| S/W Reset | Display off |
| H/W Reset | Display off |

| | |
|---|---|
| Flow Chart |  |

### 6.2.20. CASET (2Ah): Column Address Set

| 2AH | CASET (Column Address Set) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| CASET | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | (2Ah) |
| 1st Parameter | 1 | ↑ | 1 | - | XS15 | XS14 | XS13 | XS12 | XS11 | XS10 | XS9 | XS8 | |
| 2nd Parameter | 1 | ↑ | 1 | - | XS7 | XS6 | XS5 | XS4 | XS3 | XS2 | XS1 | XS0 | |
| 3rd Parameter | 1 | ↑ | 1 | - | XE15 | XE14 | XE13 | XE12 | XE11 | XE10 | XE9 | XE8 | |
| 4th Parameter | 1 | ↑ | 1 | - | XE7 | XE6 | XE5 | XE4 | XE3 | XE2 | XE1 | XE0 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

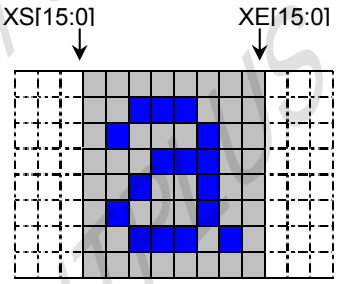
-This command is used to define area of frame memory where MCU can access.

-This command makes no change on the other driver status.

-The value of XS [15:0] and XE [15:0] are referred when RAMWR command comes.

-Each value represents one column line in the Frame Memory.

(Example)




**Restriction**

XS [15:0] always must be equal to or less than XE [15:0]

When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored.

240X320 memory base

(Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 239 (00EFh)): MV="0"

(Parameter range: 0 ≤ XS [15:0] ≤ XE [15:0] ≤ 319 (013Fh)): MV="1"

**Register Availability**

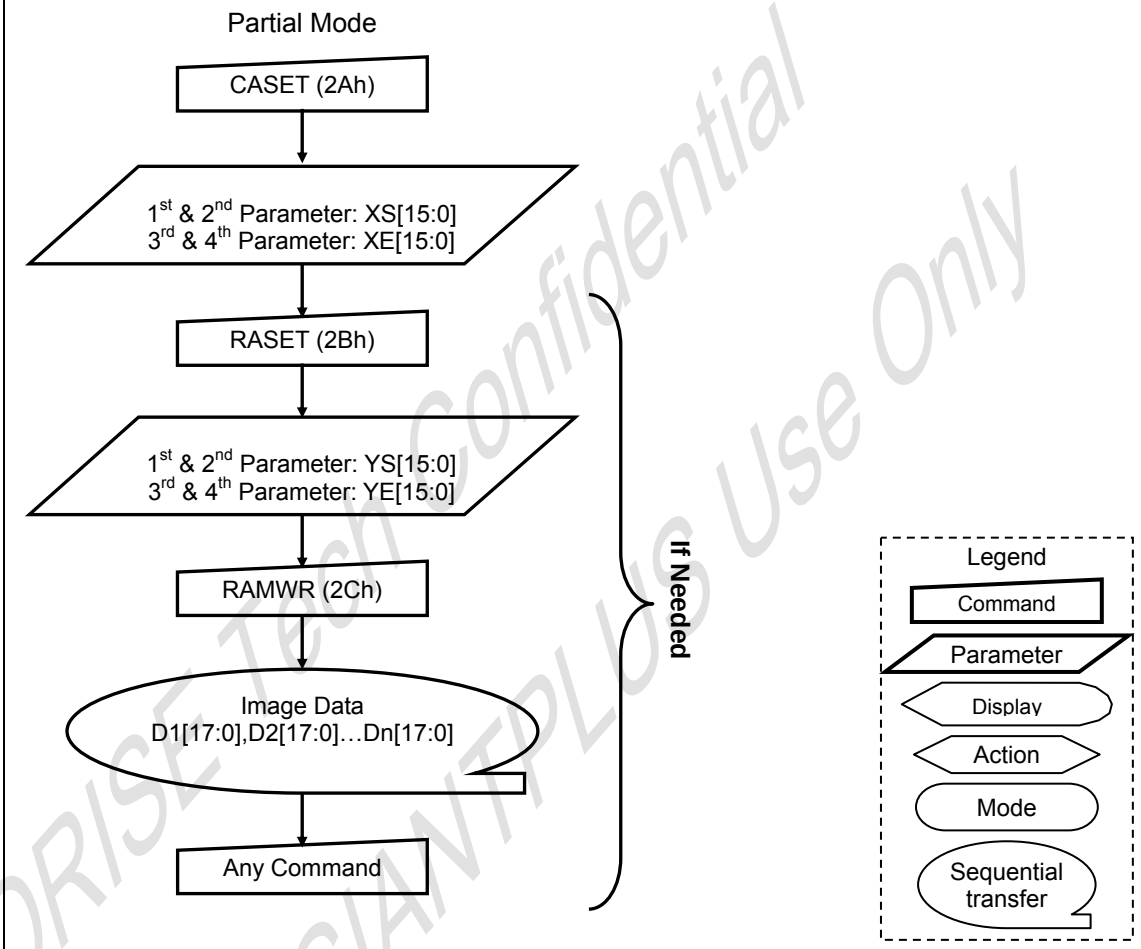
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

240x320 memory base

| Status | Default Value | | |
|---|---|---|---|
| | XS [15:0] | XE [15:0] (MV='**0**') | XE [15:0] (MV='**1**') |
| Power On Sequence | 0000h | 00EFh (239) | |
| S/W Reset | 0000h | 007Fh (2E9) | 013Fh (319) |
| H/W Reset | 0000h | 00EFh (239) | |

Flow Chart



### 6.2.21. RASET (2Bh): Row Address Set

| 2BH | RASET (Row Address Set) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| RASET (2Bh) | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | (2Bh) |
| 1st Parameter | 1 | ↑ | 1 | - | YS15 | YS14 | YS13 | YS12 | YS11 | YS10 | YS9 | YS8 | |
| 2nd Parameter | 1 | ↑ | 1 | - | YS7 | YS6 | YS5 | YS4 | YS3 | YS2 | YS1 | YS0 | |
| 3rd Parameter | 1 | ↑ | 1 | - | YE15 | YE14 | YE13 | YE12 | YE11 | YE10 | YE9 | YE8 | |
| 4th Parameter | 1 | ↑ | 1 | - | YE7 | YE6 | YE5 | YE4 | YE3 | YE2 | YE1 | YE0 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

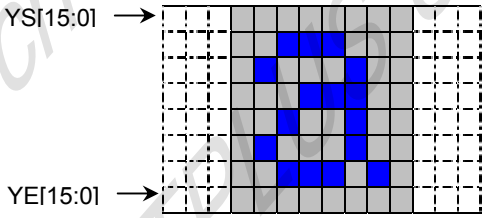
This command is used to define area of frame memory where MCU can access.

This command makes no change on the other driver status.

The value of YS [15:0] and YE [15:0] are referred when RAMWR command comes.

Each value represents one column line in the Frame Memory.

(Example)




**Restriction**

YS [15:0] always must be equal to or less than YE [15:0]

When YS [15:0] or YE [15:0] are greater than maximum row address like below, data of out of range will be ignored.

240X320 memory base

(Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 319 (013Fh)): MV="0"

(Parameter range: 0 ≤ YS [15:0] ≤ YE [15:0] ≤ 239 (0EFh)): MV="1"

**Register Availability**

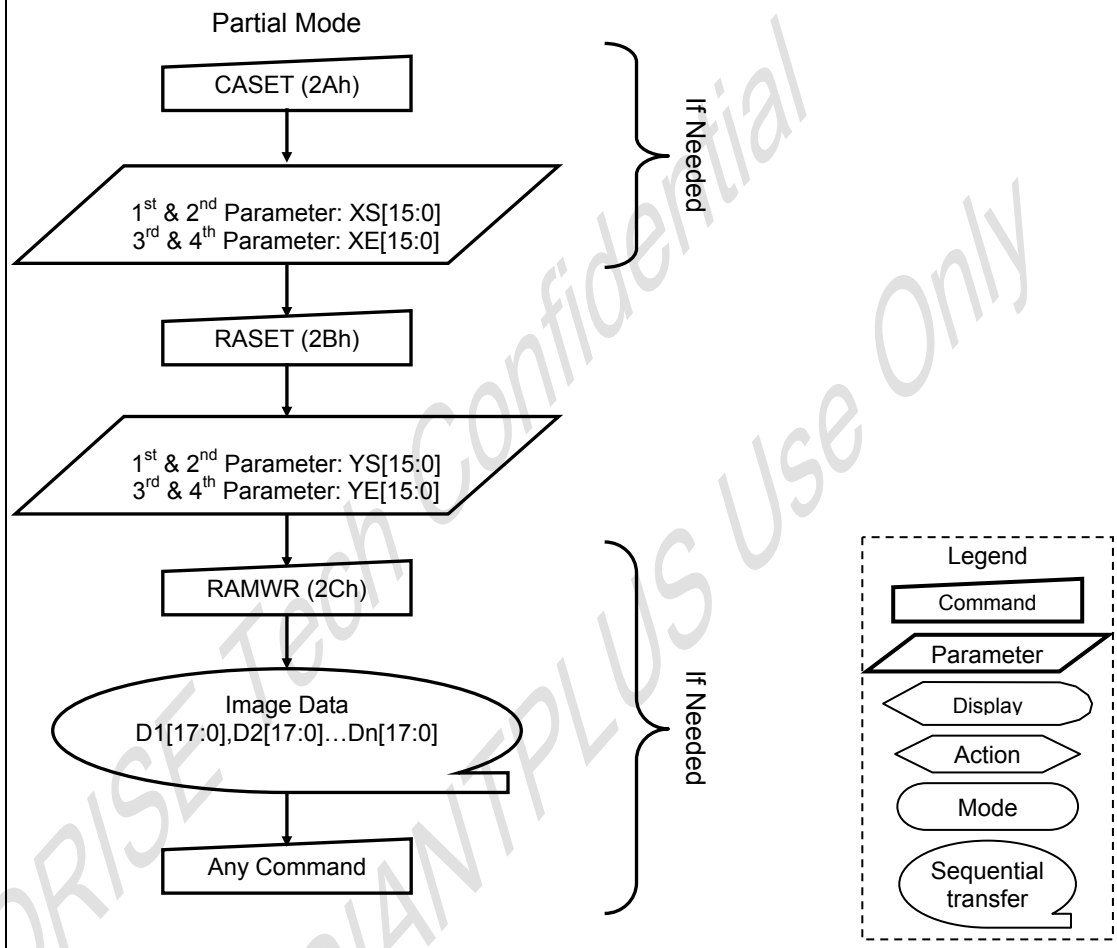
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

240x320 memory base

| Status | Default Value | | |
|---|---|---|---|
| | YS [15:0] | YE [15:0] (MV='**0**') | YE [15:0] (MV='**1**') |
| Power On Sequence | 0000h | 013Fh (319) | |
| S/W Reset | 0000h | 013Fh (319) | 00EFh (239) |
| H/W Reset | 0000h | 013Fh (319) | |

Flow Chart



### 6.2.22. RAMWR (2Ch): Memory Write

| 2CH | RAMWR (Memory Write) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| RAMWR | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | (2Ch) |
| 1st Parameter | 1 | ↑ | 1 | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | - |
| \| | 1 | ↑ | 1 | \| | \| | \| | \| | \| | \| | \| | \| | \| | \| |
| Nth Parameter | 1 | ↑ | 1 | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | - |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-This command is used to transfer data from MCU to frame memory.

-This command makes no change to the other driver status.

-When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.

-The Start Column/Start Row positions are different in accordance with MADCTR setting.

-Sending any other command can stop Frame Write.

**Restriction**

In all color modes, there is no restriction on length of parameters.

240X320 memory base

240x320x18-bit memory can be written by this command

Memory range: (0000h,0000h) -> (00EFh, 013Fh)

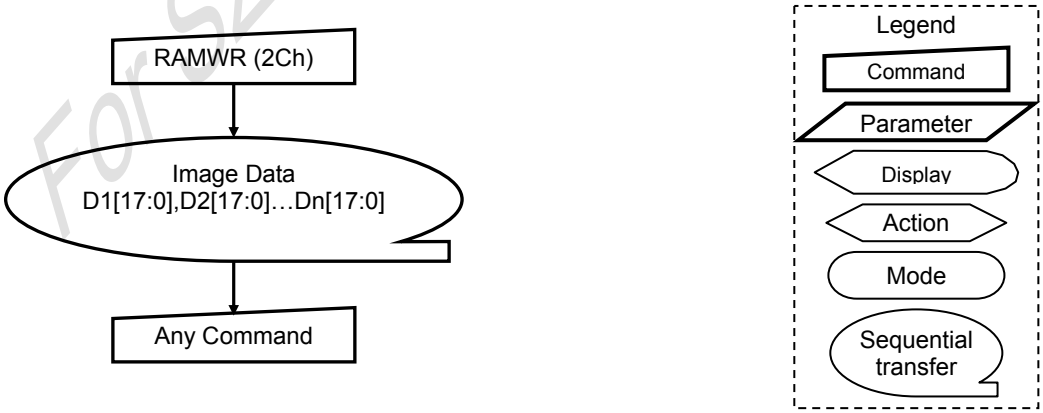
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Contents of memory is set randomly |
| S/W Reset | Contents of memory is not cleared |
| H/W Reset | Contents of memory is not cleared |

**Flow Chart**



### 6.2.23. RGBSET (2Dh): Colour Setting for 4K, 65K and 262K

| 2DH | RGBSET (Colour Set for 4K, 65K and 262K) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| RGBSET | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | (2Dh) |
| 1st Parameter | 1 | ↑ | 1 | - | - | - | R005 | R004 | R003 | R002 | R001 | R000 | - |
| \| | 1 | ↑ | 1 | - | - | - | Rnn5 | Rnn4 | Rnn3 | Rnn2 | Rnn1 | Rnn0 | - |
| \| | 1 | ↑ | 1 | - | - | - | R315 | R314 | R313 | R312 | R311 | R310 | - |
| \| | 1 | ↑ | 1 | - | - | - | G005 | G004 | G003 | G002 | G001 | G000 | - |
| \| | 1 | ↑ | 1 | - | - | - | Gnn5 | Gnn4 | Gnn3 | Gnn2 | Gnn1 | Gnn0 | - |
| \| | 1 | ↑ | 1 | - | - | - | G635 | G634 | G633 | G632 | G631 | G630 | - |
| \| | 1 | ↑ | 1 | - | - | - | B005 | B004 | B003 | B002 | B001 | B000 | - |
| \| | 1 | ↑ | 1 | - | - | - | Bnn5 | Bnn4 | Bnn3 | Bnn2 | Bnn1 | Bnn0 | - |
| 128nd Parameter | 1 | ↑ | 1 | - | - | - | B315 | B314 | B313 | B312 | B311 | B310 | - |

*NOTE: "-" Don't care, can be set to VDDIO or DGND level*

**Description**

This command is used to define the LUT for 12bits-to-16bits / 16-bits-to-18bits color depth conversations.
128-Bytes must be written to the LUT regardless of the color mode..
In this condition, 4K-color (4-4-4) and 65K-color(5-6-5) data input are transferred 6(R)-6(G)-6(B) through RGB LUT table.
This command has no effect on other commands/parameters and Contents of frame memory.
Visible change takes effect next time the Frame Memory is written to.

**Restriction**

Do not send any command before the last data is sent or LUT is not defined correctly.

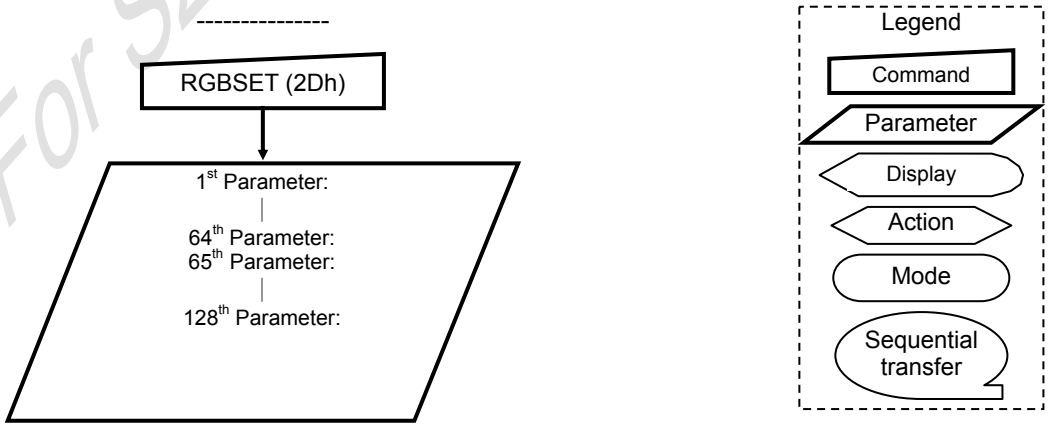
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Random |
| S/W Reset | Contents of the look-up table protected |
| H/W Reset | Random |

**Flow Chart**



### 6.2.24. RAMHD (2Eh): Memory Read

| 2EH | RAMHD (Memory Read) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| RAMHD | 0 | ↑ | 1 | - | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | (2Eh) |
| 1st Parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd Parameter | 1 | 1 | ↑ | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | - |
| \| | 1 | 1 | ↑ | \| | \| | \| | \| | \| | \| | \| | \| | \| | \| |
| (N+1)th Parameter | 1 | 1 | ↑ | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | - |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-This command is used to transfer data from frame memory to MCU.

-This command makes no change to the other driver status.

-When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.

-The Start Column/Start Row positions are different in accordance with MADCTR setting.

-Frame Read can be canceled by sending any other command.

**Restriction**

-In all color modes, the Frame Read is always 18-bits and there is no restriction on length of parameters.

-Memory read is only possible via the SPI and parallel interface.

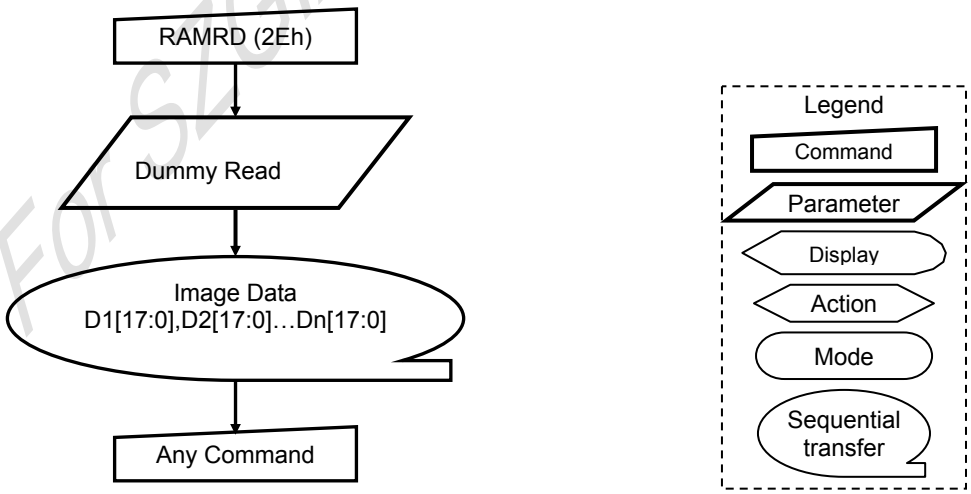
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Contents of memory is set randomly |
| S/W Reset | Contents of memory is not cleared |
| H/W Reset | Contents of memory is not cleared |

**Flow Chart**



### 6.2.25. PTLAR (30h): Partial Area

| 30H | PTLAR (Partial Area) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| PTLAR | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | (30h) |
| 1st Parameter | 1 | ↑ | 1 | - | PSL15 | PSL14 | PSL13 | PSL12 | PSL11 | PSL10 | PSL9 | PSL8 | |
| 2nd Parameter | 1 | ↑ | 1 | - | PSL7 | PSL6 | PSL5 | PSL4 | PSL3 | PSL2 | PSL1 | PSL0 | |
| 3rd Parameter | 1 | ↑ | 1 | - | PEL15 | PEL14 | PEL13 | PEL12 | PEL11 | PEL10 | PEL9 | PEL8 | |
| 4th Parameter | 1 | ↑ | 1 | - | PEL7 | PEL6 | PEL5 | PEL4 | PEL3 | PEL2 | PEL1 | PEL0 | |

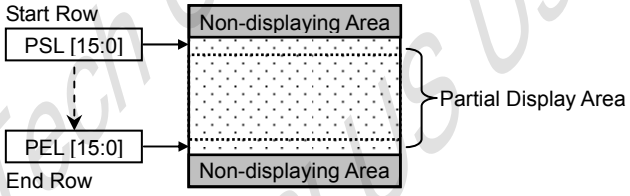
*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

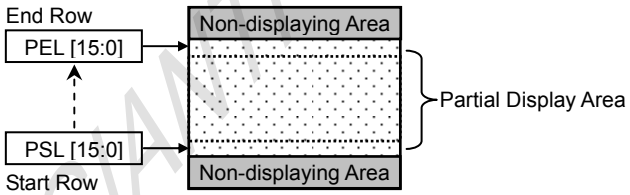
-This command defines the partial mode's display area.

-There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

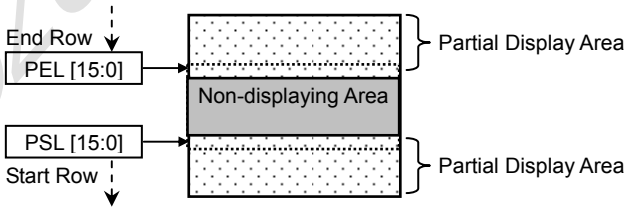
-If End Row > Start Row, when MADCTL ML='0'




-If End Row > Start Row, when MADCTL ML='1'




-If End Row < Start Row, when MADCTL ML='0'




-If End Row = Start Row then the Partial Area will be one row deep.

**Restriction**

-

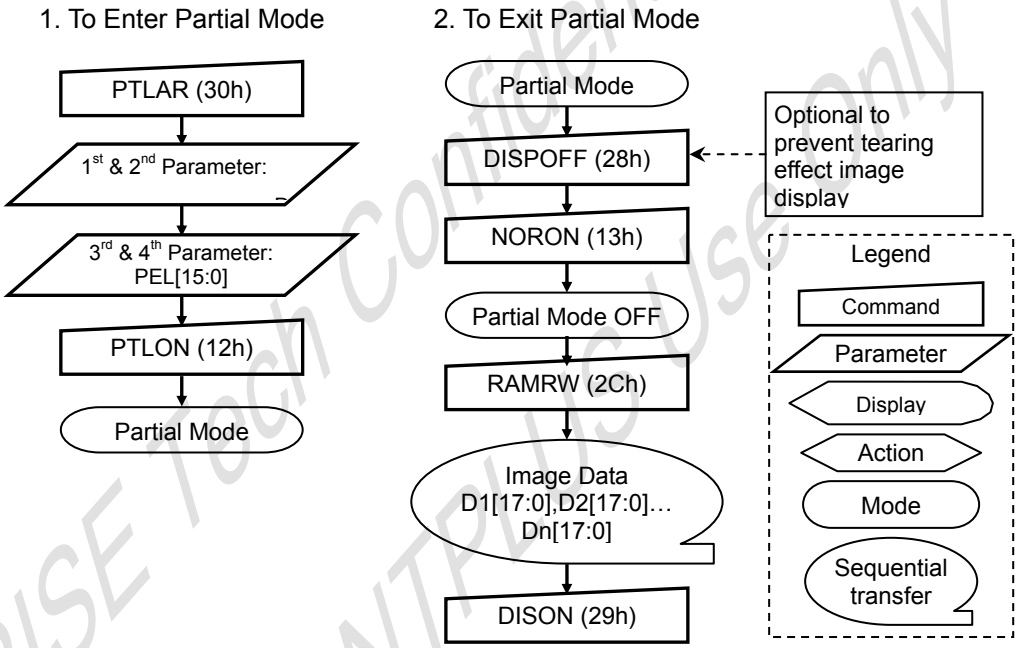
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | |
|---|---|---|
| | PSL [15:0] | PEL [15:0] |
| Power On Sequence | 0000h | 013Fh |
| S/W Reset | 0000h | 013Fh |
| H/W Reset | 0000h | 013Fh |

Flow Chart



### 6.2.26. SCRLAR (33h): Scroll Area

| 33H | SCRLAR (Scroll Area) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| SCRLAR | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | (33h) |
| 1st Parameter | 1 | ↑ | 1 | - | TFA15 | TFA14 | TFA13 | TFA12 | TFA11 | TFA10 | TFA9 | TFA8 | |
| 2nd Parameter | 1 | ↑ | 1 | - | TFA7 | TFA6 | TFA5 | TFA4 | TFA3 | TFA2 | TFA1 | TFA0 | |
| 3rd Parameter | 1 | ↑ | 1 | - | VSA15 | VSA14 | VSA13 | VSA12 | VSA11 | VSA10 | VSA9 | VSA8 | |
| 4th Parameter | 1 | ↑ | 1 | - | VSA7 | VSA6 | VSA5 | VSA4 | VSA3 | VSA2 | VSA1 | VSA0 | |
| 5th Parameter | 1 | ↑ | 1 | - | BFA15 | BFA14 | BFA13 | BFA12 | BFA11 | BFA10 | BFA9 | BFA8 | |
| 6th Parameter | 1 | ↑ | 1 | - | BFA7 | BFA6 | BFA5 | BFA4 | BFA3 | BFA2 | BFA1 | BFA0 | |

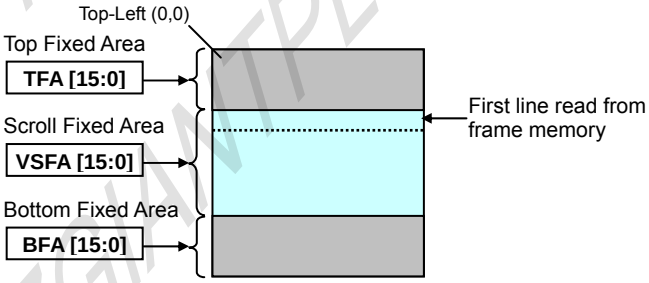
*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

This command defines the Vertical Scrolling Area of the display.

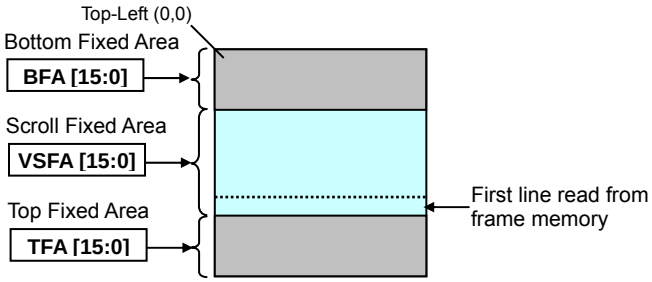
When MADCTR ML=0

- The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).
- The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)
- The first line appears immediately after the bottom most line of the Top Fixed Area.
- The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
- TFA, VSA and BFA refer to the Frame Memory row address.




When MADCTR ML=1

- The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
- The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address)
- The first line appears immediately after the top most line of the Top Fixed Area.
- The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).




**Restriction**

-The condition is 0 ≤ (TFA+VSA+BFA) ≤ 162, otherwise Scrolling mode is undefined.

-In Vertical Scroll Mode, MADCTR parameter MV should be set to '0'-this only affects the Frame Memory Write.

**Register Availability**

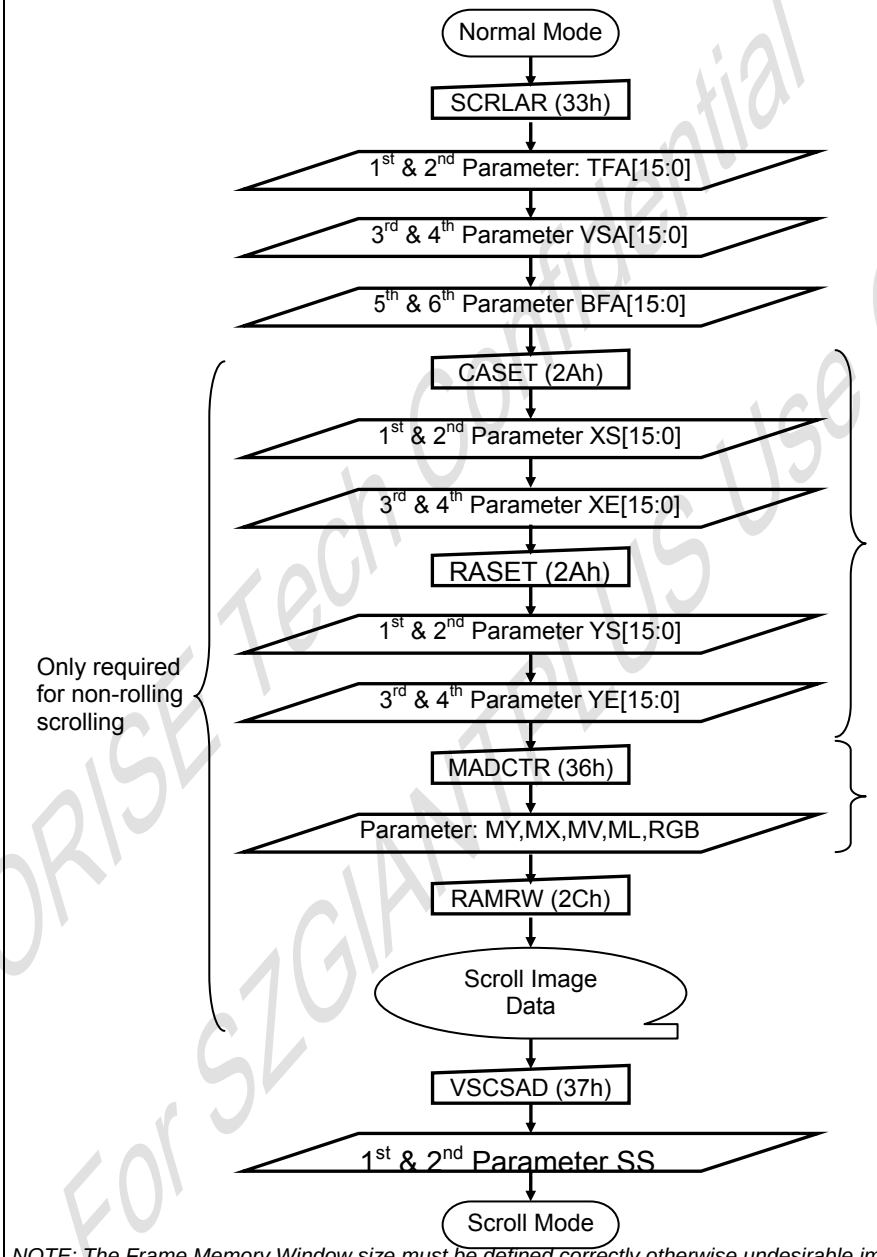
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | | |
|---|---|---|---|
| | TFA [15:0] | VSA [15:0] | BFA [15:0] |
| Power On Sequence | 0000h | 0140h | 0000h |
| S/W Reset | 0000h | 0140h | 0000h |
| H/W Reset | 0000h | 0140h | 0000h |

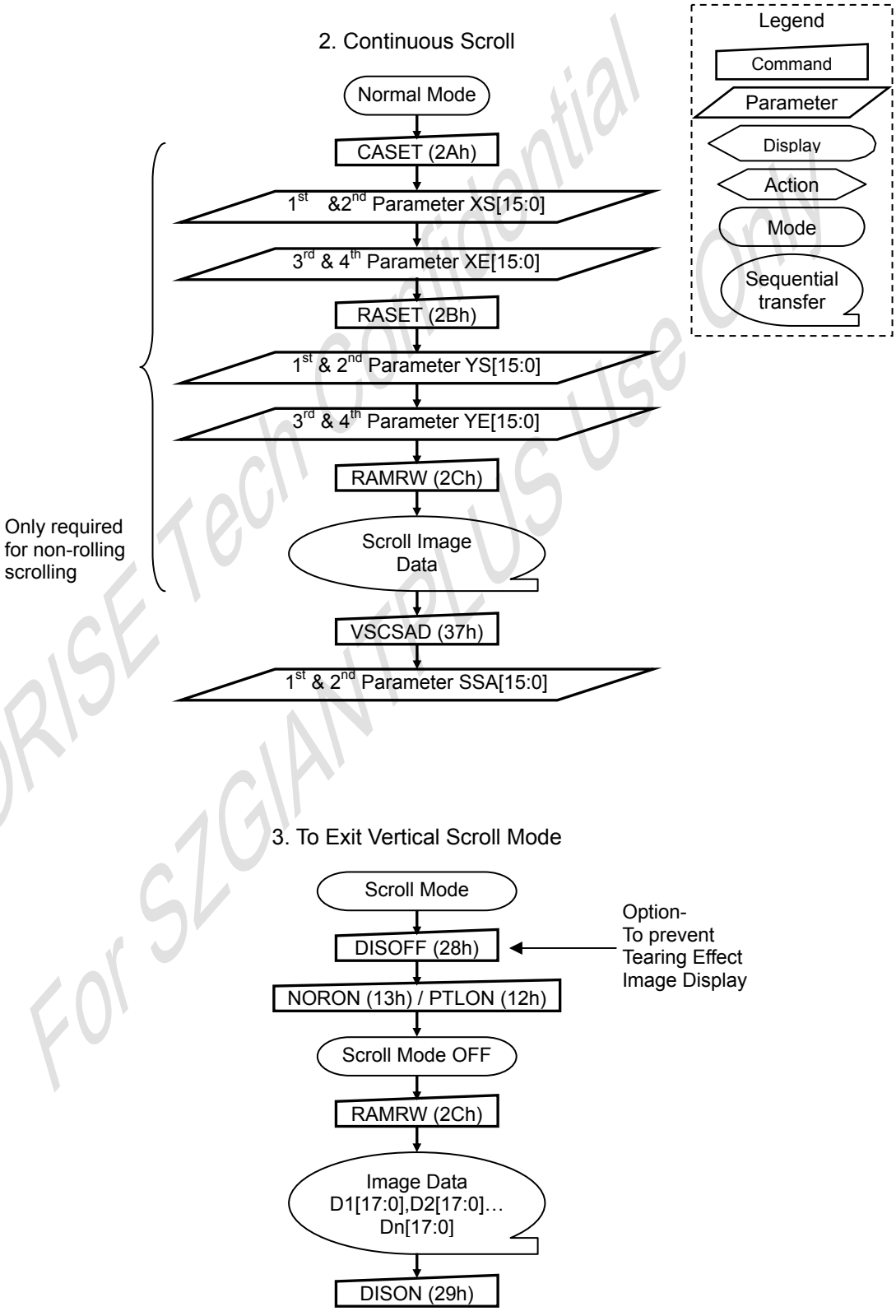
Flow Chart

1. To Enter Vertical Scroll Mode




*NOTE: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.*

Flow Chart




*NOTE: Scroll Mode can be exit by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.*

### 6.2.27. TEOFF (34h): Tearing Effect Line OFF

| 34H | TEOFF (Tearing Effect Line OFF) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| TEOFF | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | (34h) |
| 1st Parameter | No Parameter | | | | | | | | | | | | - |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

| | |
|---|---|
| Description | -This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line. |
| Restriction | -This command has no effect when Tearing Effect output is already OFF. |
| Register Availability | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | OFF |
| S/W Reset | OFF |
| H/W Reset | OFF |

Flow Chart

### 6.2.28. TEON (35h): Tearing Effect Line ON

| 35H | TEON (Tearing Effect Line ON) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| TEON | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | (35h) |
| 1st Parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TELOM | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-This command is used to turn ON the Tearing Effect output signal from the TE signal line.

-This output is not affected by changing MADCTR bit ML.

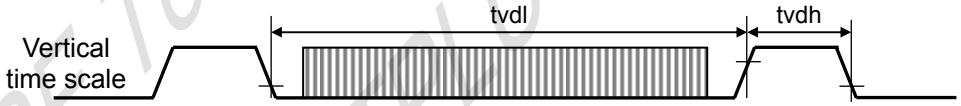
-The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-"=Don't Care).

—When M='0':

The Tearing Effect Output line consists of V-Blanking information only.


—When M='1':

The Tearing Effect Output line consists of both V-Blanking and H-Blinking information.




*Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.*

**Restriction**

-This command has no effect when Tearing Effect output is already OFF.

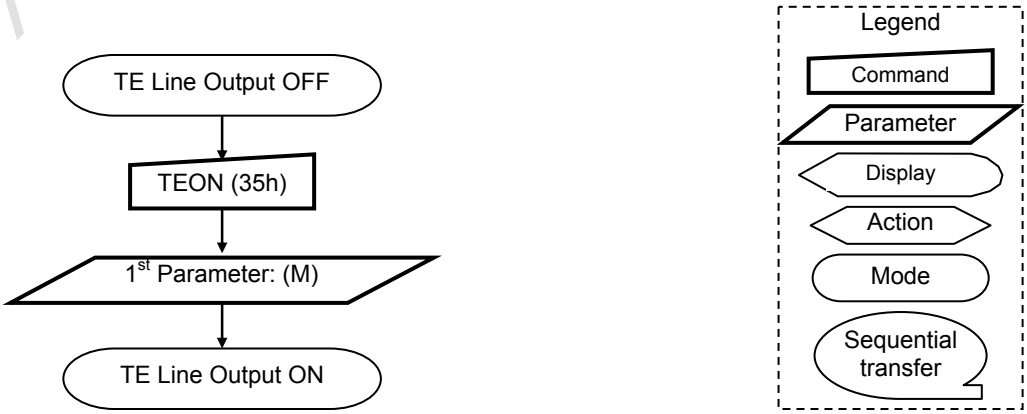
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Tearing effect off & TELOM=0 |
| S/W Reset | Tearing effect off & TELOM=0 |
| H/W Reset | Tearing effect off & TELOM=0 |

**Flow Chart**



### 6.2.29. MADCTR (36h): Memory Data Access Control

| 36H | MADCTR (Memory Data Access Control) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| MADCTR | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | (36h) |
| 1st Parameter | 1 | ↑ | 1 | - | MY | MX | MV | ML | RGB | 0 | 0 | 0 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

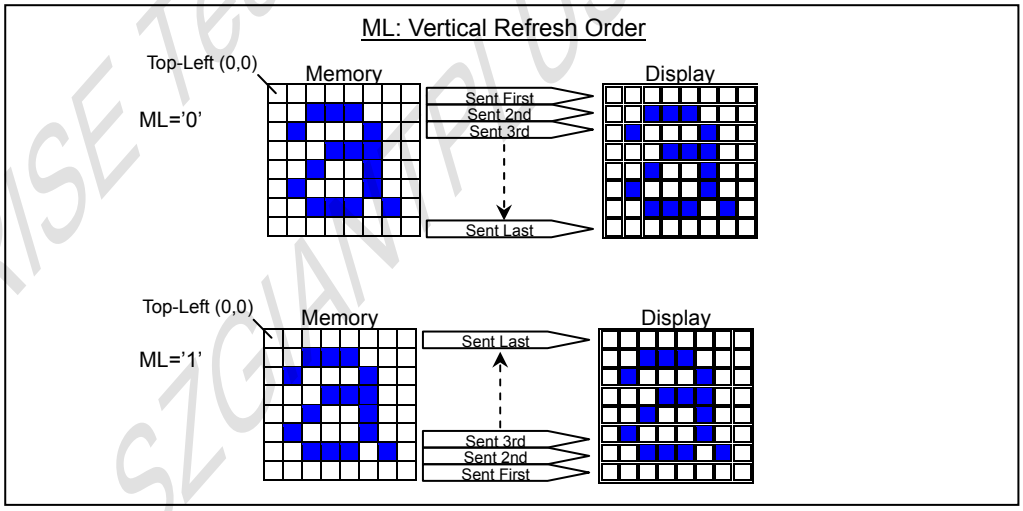
Description

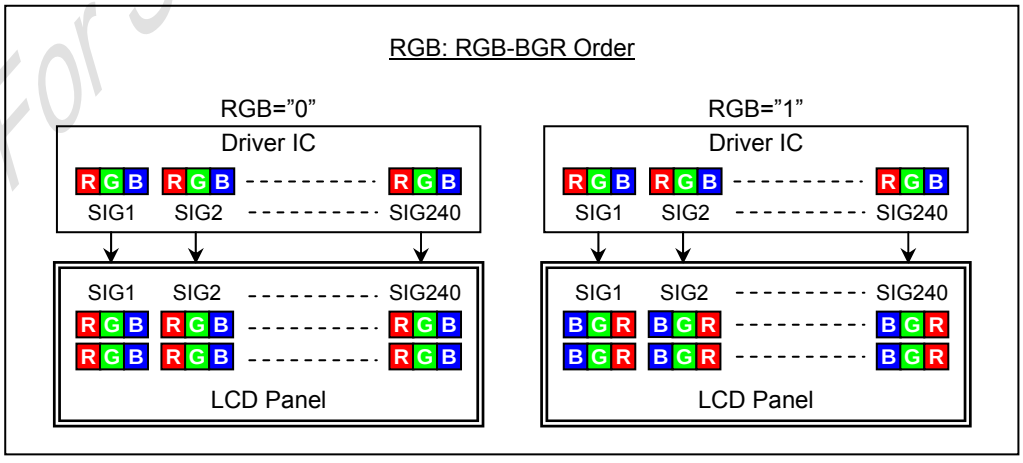
-This command defines read/ write scanning direction of frame memory.

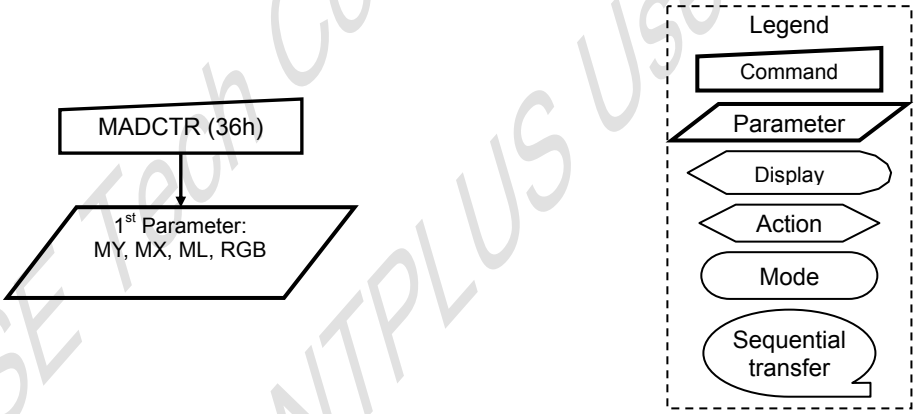
-This command makes no change on the other driver status.

-Bit Assignment

| Bit | NAME | DESCRIPTION |
|---|---|---|
| MY | Row Address Order | These 3bits controls MCU to memory write/read direction. |
| MX | Column Address Order | |
| MV | Row/Column Exchange | |
| ML | Vertical Refresh Order | LCD vertical refresh direction control<br>'0' = LCD vertical refresh Top to Bottom<br>'1' = LCD vertical refresh Bottom to Top |
| RGB | RGB-BGR ORDER | Color selector switch control<br>'0' =RGB color filter panel,<br>'1' =BGR color filter panel) |



<table>
<tr><td>Restriction</td><td>D1 and D0 of the 1st parameter are set to “00” internally.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>MY=0,MX=0,MV=0,ML=0,RGB=0</td></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>MY=0,MX=0,MV=0,ML=0,RGB=0</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

### 6.2.30. VSCSAD (37h): Vertical Scroll Start Address of RAM

| 37H | VSCSAD (Vertical Scroll Start Address of RAM) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| VSCSAD | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | (37h) |
| 1st Parameter | 1 | ↑ | 1 | - | SSA15 | SSA14 | SSA13 | SSA12 | SSA11 | SSA10 | SSA9 | SSA8 | |
| 2nd Parameter | 1 | ↑ | 1 | - | SSA7 | SSA6 | SSA5 | SSA4 | SSA3 | SSA2 | SSA1 | SSA0 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.

-The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

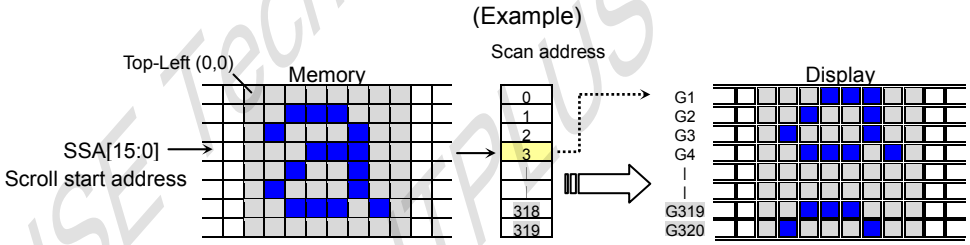
-This command Start the scrolling.

-Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h).

**When MADCTR ML= '0'**

Example:

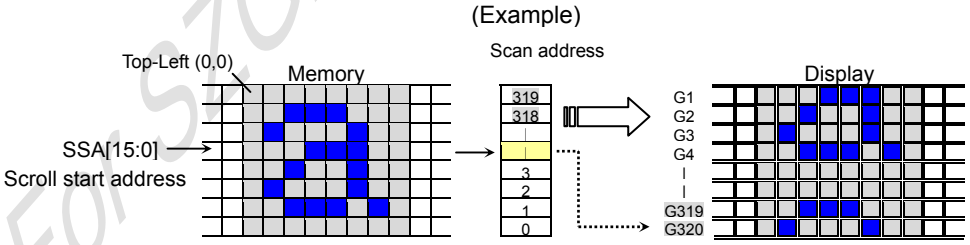
—When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=320 and Vertical Scrolling Pointer SSA= '3'.




**When MADCTR ML = '1'**

Example:

—When Top Fixed Area= Bottom Fixed Area=00, Vertical Scrolling Area=320 and SSA= '3'




*NOTE: -When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.*
*-SSA refers to the Frame Memory scan address.*

**Restriction**

-Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)-otherwise undesirable image will be displayed on the Panel.

SSA[15:0] is based on 1-line unit.

-SSA[15:0] = 0000h, 0001h, 0002h, 0003h, … , 0013Fh

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td></tr>
<tr><td>S/W Reset</td><td>0000h</td></tr>
<tr><td>H/W Reset</td><td>0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

### 6.2.31. IDMOFF (38h): Idle Mode Off

| 38H | IDMOFF (Idle Mode Off) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| IDMOFF | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | (38h) |
| 1st Parameter | No Parameter | | | | | | | | | | | | - |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

| | |
|---|---|
| Description | -This command is used to recover from Idle mode on.<br>-There will be no abnormal visible effect on the display mode change transition.<br>-In the idle off mode,<br>1. LCD can display 4096, 65k or 262k colors.<br>2. Normal frame frequency is applied. |
| Restriction | -This command has no effect when module is already in idle off mode. |
| Register Availability | Status: Availability<br>Normal Mode On, Idle Mode Off, Sleep Out: Yes<br>Normal Mode On, Idle Mode On, Sleep Out: Yes<br>Partial Mode On, Idle Mode Off, Sleep Out: Yes<br>Partial Mode On, Idle Mode On, Sleep Out: Yes<br>Sleep In: Yes |
| Default | Status: Default Value<br>Power On Sequence: Idle Mode Off<br>S/W Reset: Idle Mode Off<br>H/W Reset: Idle Mode Off |
| Flow Chart |  |

### 6.2.32. IDMON (39h): Idle Mode On

| 39H | IDMON (Idle Mode On) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| IDMON | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | (39h) |
| 1st Parameter | No Parameter | | | | | | | | | | | | - |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

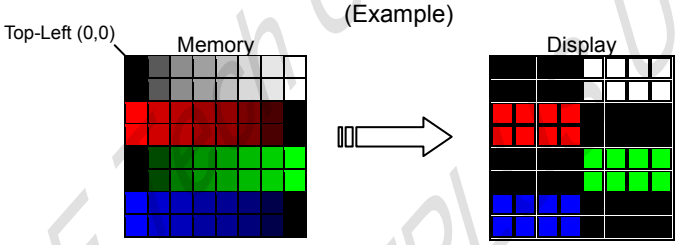
-This command is used to enter into Idle mode on.

-There will be no abnormal visible effect on the display mode change transition.

-In the idle on mode,

1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command

(Example)




| Color | $R_5 R_4 R_3 R_2 R_1 R_0$ | $G_5 G_4 G_3 G_2 G_1 G_0$ | $B_5 B_4 B_3 B_4 B_1 B_0$ |
|---|---|---|---|
| Black | 0xxxxx | 0xxxxx | 0xxxxx |
| Blue | 0xxxxx | 0xxxxx | 1xxxxx |
| Red | 1xxxxx | 0xxxxx | 0xxxxx |
| Magenta | 1xxxxx | 0xxxxx | 1xxxxx |
| Green | 0xxxxx | 1xxxxx | 0xxxxx |
| Cyan | 0xxxxx | 1xxxxx | 1xxxxx |
| Yellow | 1xxxxx | 1xxxxx | 0xxxxx |
| White | 1xxxxx | 1xxxxx | 1xxxxx |

**Restriction**

This command has no effect when module is already in idle on mode.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Idle Mode Off |
| S/W Reset | Idle Mode Off |
| H/W Reset | Idle Mode Off |

| | |
|---|---|
| Flow Chart |  |

### 6.2.33. COLMOD (3Ah): Interface Pixel Format

| 3AH | COLMOD (3Ah): Interface Pixel Format | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| COLMOD | 0 | ↑ | 1 | - | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | (3Ah) |
| 1st Parameter | 1 | ↑ | 1 | - | - | - | - | - | - | IFPF2 | IFPF1 | IFPF0 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface. The formats are shown in the table:

| IFPF[2:0] | | MCU Interface Color Format |
|---|---|---|
| 011 | 3 | 12-bits/pixel |
| 101 | 5 | 16-bits/pixel |
| 110 | 6 | 18-bits/pixel |
| 111 | 7 | No used |

Others are no define and invalid

*Note1: In 12-bits/Pixel, 16-bits/Pixel or 18-bits/Pixel mode, the LUT is applied to transfer data into the Frame Memory.*

**Restriction**

There is no visible effect until the Frame Memory is written to.

**Register Availability**

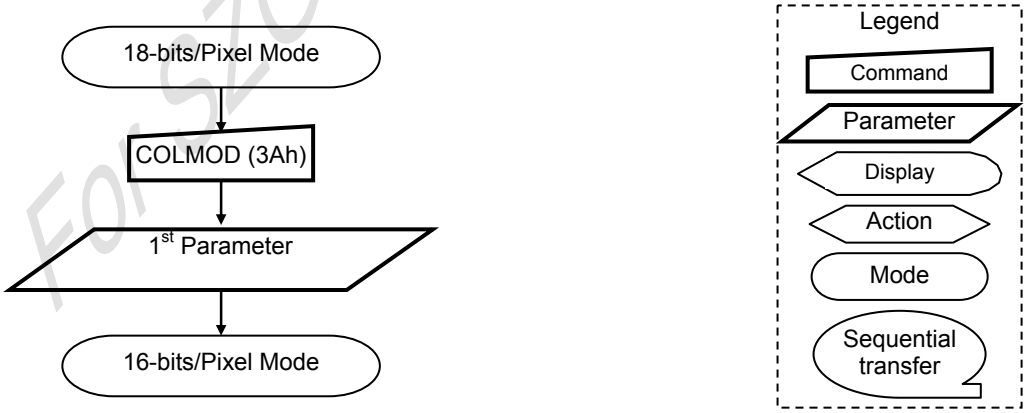
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| | IFPF[2:0] |
| Power On Sequence | 0110 (18-bits/pixel) |
| S/W Reset | No Change |
| H/W Reset | 0110 (18-bits/pixel) |

**Flow Chart**

Example:



### 6.2.34. RDID1 (DAh): Read ID1 Value

| DAH | RDID1 (Read ID1 Value) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| RDID1 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | (DAh) |
| 1st Parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd Parameter | 1 | 1 | ↑ | - | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-This read byte returns 8-bits LCD module's manufacturer ID

-The 1st parameter is dummy data

-The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.

*NOTE: See command RDDID (04h), 2nd parameter.*

**Restriction**

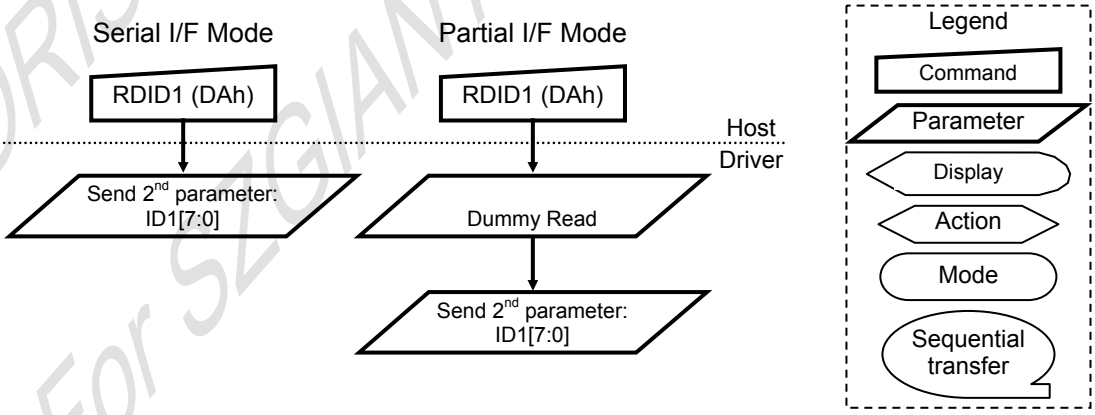
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 38h |
| S/W Reset | 38h |
| H/W Reset | 38h |

**Flow Chart**



### 6.2.35. RDID2 (DBh): Read ID2 Value

| DBH | RDID2 (Read ID2 Value) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| RDID2 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | (DBh) |
| 1st Parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd Parameter | 1 | 1 | ↑ | - | ID27 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-This read byte returns 8-bits LCD module/driver version ID

-The 1st parameter is dummy data

-The 2nd parameter (ID26 to ID20): LCD module/driver version ID

-Parameter Range: ID=80h to FFh

| ID26 to ID20 | Version | Changes |
|---|---|---|
| 80h | | |
| 81h | | |
| 82h | | |
| 83h | | |
| - | | |

*NOTE: See command RDDID (04h), 3rd parameter.*

**Restriction**

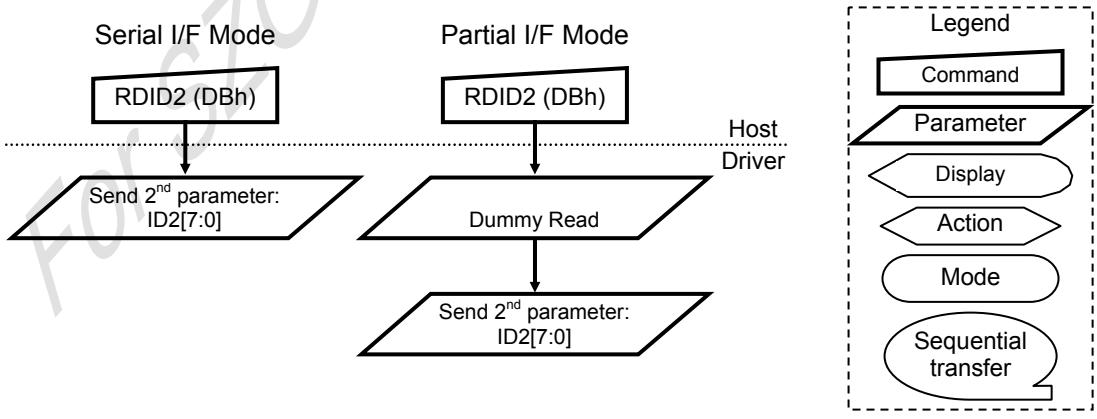
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 80h |
| S/W Reset | 80h |
| H/W Reset | 80h |

**Flow Chart**



### 6.2.36. RDID3 (DCh): Read ID3 Value

| DCH | RDID3 (Read ID2 Value) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| RDID3 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | (DCh) |
| 1st Parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd Parameter | 1 | 1 | ↑ | - | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-This read byte returns 8-bits LCD module/driver ID.

-The 1st parameter is dummy data

-The 2nd parameter (ID37 to ID30): LCD module/driver ID.

*NOTE: See command RDDID (04h), 4th parameter.*

**Restriction**

-

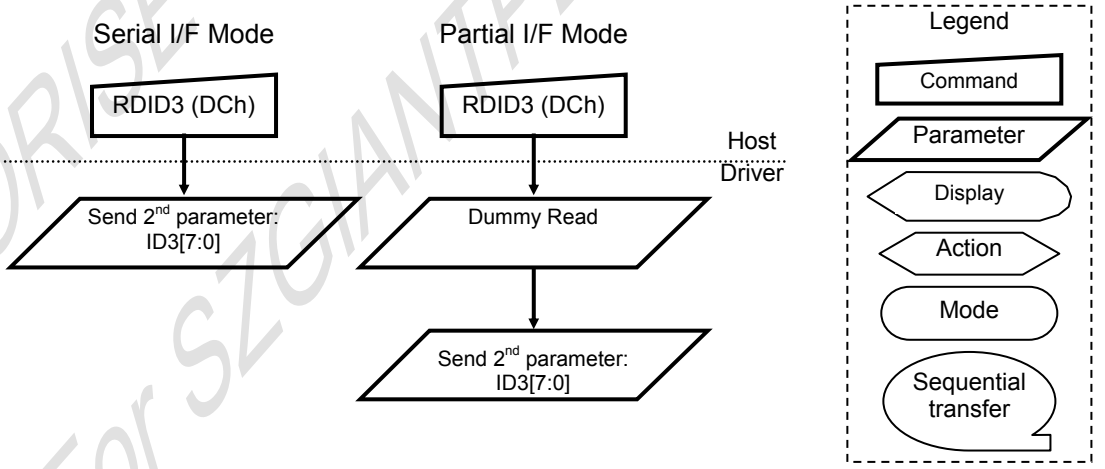
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 4Fh |
| S/W Reset | 4Fh |
| H/W Reset | 4Fh |

**Flow Chart**



### 6.2.37. WRDISBV (51h): Write Display Brightness

| 51H | WRDISBV (Write Display Brightness) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 51 |
| Parameter | 1 | 1 | ↑ | DBV 7 | DBV 6 | DBV 5 | DBV 4 | DBV 3 | DBV 2 | DBV 1 | DBV 0 | 00 .. FF |
| Description | This command is used to adjust the brightness value of the display.<br>It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification.<br>In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | |

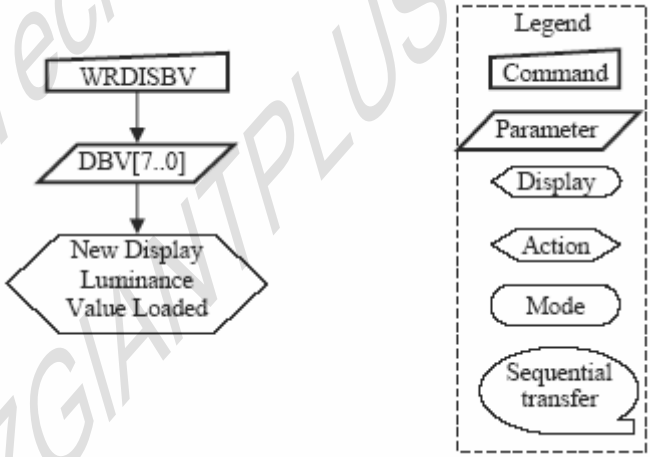
Register Availability

| Status | Availability |
|---|---|
| Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

Flow Chart



### 6.2.38. RDDISBV(52h):Read Display Brightness Value

| 52H | RDDISBV (Read Display Brightness Value) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 52 |
| 1 st parameter | 1 | ↑ | 1 | xx | xx | xx | xx | xx | xx | xx | xx | Xx |
| 2 nd parameter | 1 | ↑ | 1 | DBV 7 | DBV 6 | DBV 5 | DBV 4 | DBV 3 | DBV 2 | DBV 1 | DBV 0 | Xx |

**Description**

This command is used to adjust the brightness value of the display.
It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is.
In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.
See chapters: "6.2.37 Write Display Brightness (51h)"
This command can be used to read the brightness value of the display also when Display brightness control is in automatic mode. See chapter "6.2.39 Write CTRL Display (53h)" bit DB = '1'.
DBV [7:0] is reset when display is in sleep-in mode.
DBV [7:0] is '0' when bit BCTRL of "6.2.39 Write CTRL Display (53h)" command is '0'.
DBV [7:0] is manual set brightness specified with "6.2.39 Write CTRL Display (53h) command when bit BCTRL is '1' and bit A of "6.2.39 Write CTRL Display (53h)" command is '0'.

When bit BCTRL of "6.2.39 Write CTRL Display (53h)" command is '1' and bit C1/C0 of "6.2.41 Write Content Adaptive Brightness Control (55h)" are '0', DBV[7:0] output is the brightness value specified with "6.2.37 Write Display Brightness (51h)" command.

**Restrictions**

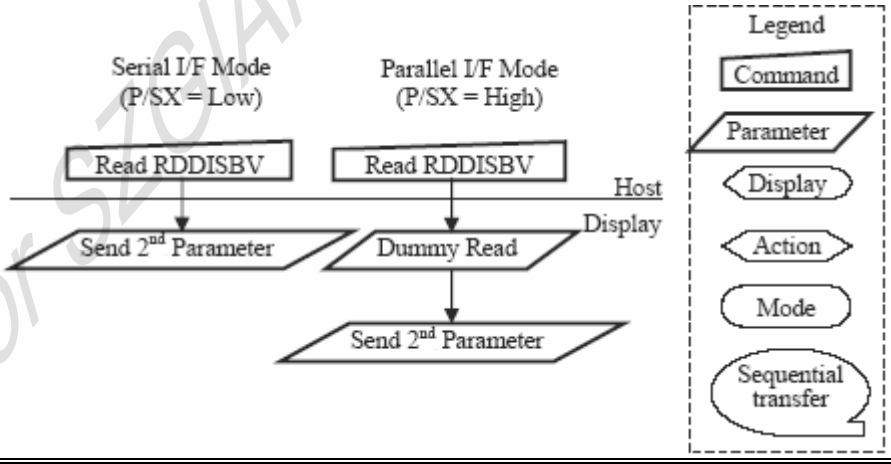
**Register Availability**

| Status | Availability |
|---|---|
| Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | $00_{HEX}$ |
| S/W Reset | $00_{HEX}$ |
| H/W Reset | $00_{HEX}$ |

**Flow Chart**



### 6.2.39. WRCTRLD(53h) : Write CTRL Display

| 53H | WRCTRLD (Write Control Display) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 53 |
| Parameter | 1 | 1 | ↑ | X | X | BCTRL | X | DD | BL | X | X | 00 .. FF |

**Description**

This command is used to control ambient light, brightness and gamma settings.

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display and keyboard.
0 = Off (Brightness registers are 00h, DBV[7..0] and KBV[7..0])
1 = On (Brightness registers are active, according to the other parameters.)

Display Dimming (DD):
DD = 0: Display Dimming is off
DD = 1: Display Dimming is on

BL: Backlight Control On/Off
0 = Off (Completely turn off backlight circuit. Control lines must be low. )
1 = On

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0.

When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.

X = Don’t care.

**Restriction**

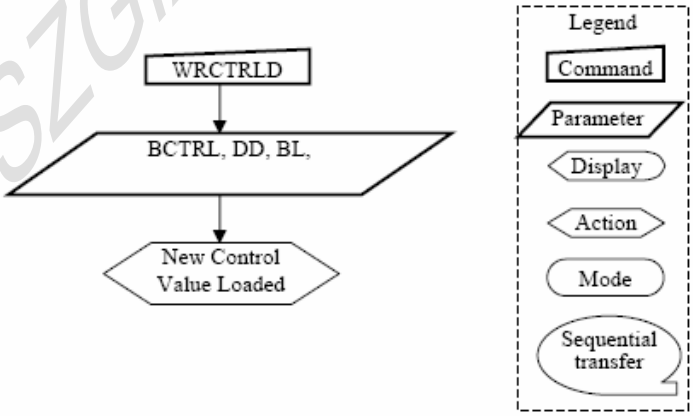
**Register Availability**

| Status | Availability |
|---|---|
| Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

**Flow Chart**



### 6.2.40. RDCTRLD (54h) : Read CTRL Value Display

| 54H | RDCTRLD (Read Control Value Display) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 54 |
| 1 st parameter | 1 | ↑ | 1 | xx | xx | xx | xx | xx | xx | xx | xx | xx |
| 2 nd parameter | 1 | ↑ | 1 | 0 | 0 | BCTRL | 0 | DD | BL | 0 | 0 | xx |

**Description**

This command returns ambient light and brightness control values, see chapter: "6.2.39 Write CTRL Display (53h)".

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display and keyboard.
0 = Off
1 = On

Display Dimming (DD):
DD = 0: Display Dimming is off
DD = 1: Display Dimming is on

BL: Backlight Control On/Off
0 = Off (completely turn off backlight circuit)
1 = On

**Restrictions**

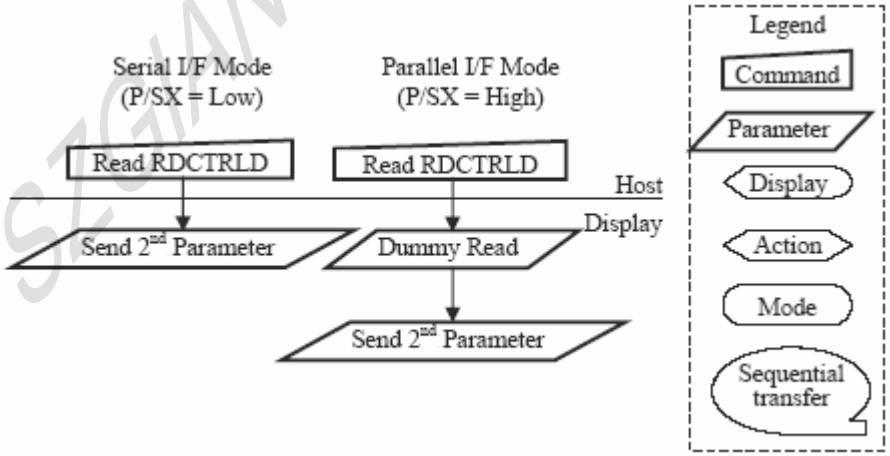
**Register Availability**

| Status | Availability |
|---|---|
| Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | $00_{HEX}$ |
| S/W Reset | $00_{HEX}$ |
| H/W Reset | $00_{HEX}$ |

**Flow Chart**



### 6.2.41. WRCABC (55h): Write Content Adaptive Brightness Control

| 55H | WRCABC (Write Content Adaptive Brightness Control) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 55 |
| 1 st Parameter | 1 | 1 | ↑ | X | X | X | X | X | X | C1 | C0 | xx |

**Description**

This command is used to set parameters for image content based adaptive brightness control functionality.
There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

| C1 | C0 | Function | Note |
|---|---|---|---|
| 0 | 0 | Off | |
| 0 | 1 | User Interface Image | |
| 1 | 0 | Still Picture | |
| 1 | 1 | Moving Image | |

X = Don't care.

**Restriction**

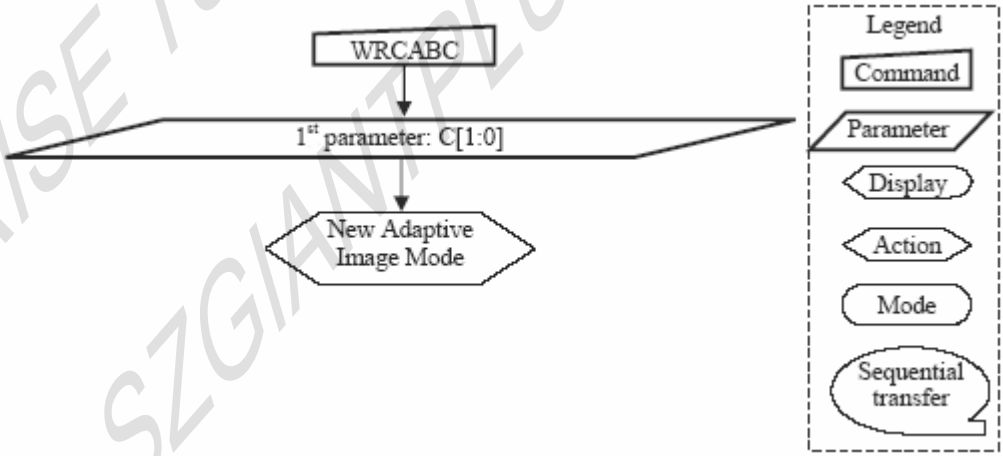
**Register Availability**

| Status | Availability |
|---|---|
| Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

**Flow Chart**



### 6.2.42. RDCABC (56h) : Read Content Adaptive Brightness Control

| 56H | RDCABC (Read Content Adaptive Brightness Control) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 56 |
| 1 st parameter | 1 | ↑ | 1 | xx | xx | Xx | xx | xx | xx | xx | Xx | Xx |
| 2 nd parameter | 1 | ↑ | 1 | 0 | 0 | 0 | 0 | 0 | 0 | C1 | C0 | Xx |

**Description**

This command is used to read the settings for image content based adaptive brightness control functionality
There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

| C1 | C0 | Function | Note |
|---|---|---|---|
| 0 | 0 | Off | |
| 0 | 1 | User Interface Image | |
| 1 | 0 | Still Picture | |
| 1 | 1 | Moving Image | |

**Restrictions**

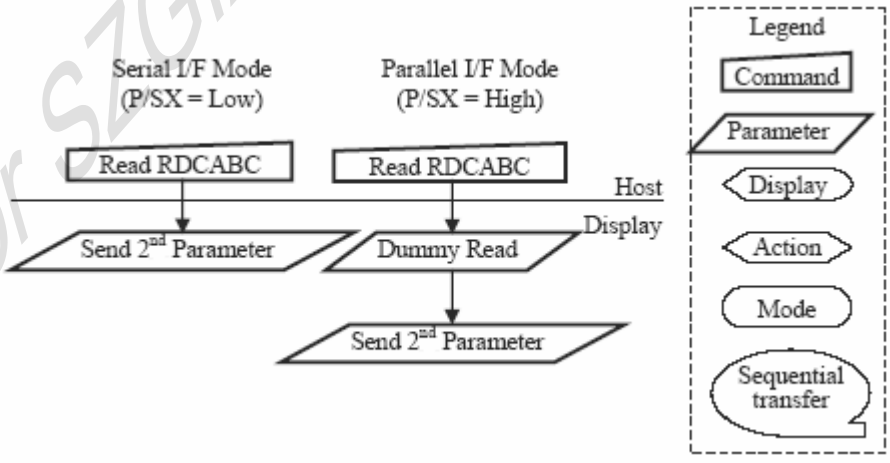
**Register Availability**

| Status | Availability |
|---|---|
| Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | $00_{HEX}$ |
| S/W Reset | $00_{HEX}$ |
| H/W Reset | $00_{HEX}$ |

**Flow Chart**



### 6.2.43. WRCABCMB (5Eh) :Write CABC minimum brightness

| 5EH | WRCABCMB (Write CABC minimum brightness) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 5E |
| Parameter | 1 | 1 | ↑ | CMB 7 | CMV 6 | CMB 5 | CMB 4 | CMB 3 | CMB 2 | CMB 1 | CMB 0 | 00 .. FF |
| Description | This command is used to set the minimum brightness value of the display for CABC function.<br>In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. | | | | | | | | | | | |
| Restriction | - | | | | | | | | | | | |

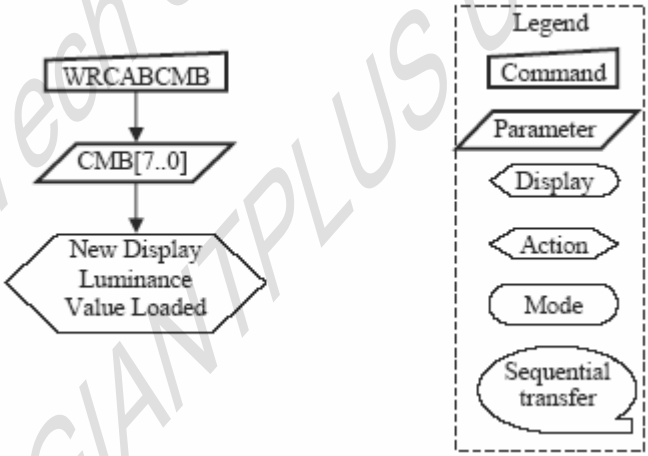
Register Availability

| Status | Availability |
|---|---|
| Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |

Flow Chart



### 6.2.44. RDCABCMB (5Fh) : Read CABC minimum brightness

| 5FH | RDCABCMB (Read CABC minimum brightness) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 5F |
| 1 st parameter | 1 | ↑ | 1 | xx | xx | xx | xx | xx | xx | xx | xx | Xx |
| 2 nd parameter | 1 | ↑ | 1 | CMB 7 | CMB 6 | CMB 5 | CMB 4 | CMB 3 | CMB 2 | CMB 1 | CMB 0 | Xx |
| Description | This command returns the minimum brightness value of CABC function.<br>In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.<br>CMB[7:0] is CABC minimum brightness specified with “6.2.43 Write CABC minimum brightness (5Eh)” command. | | | | | | | | | | | |
| Restrictions | | | | | | | | | | | | |

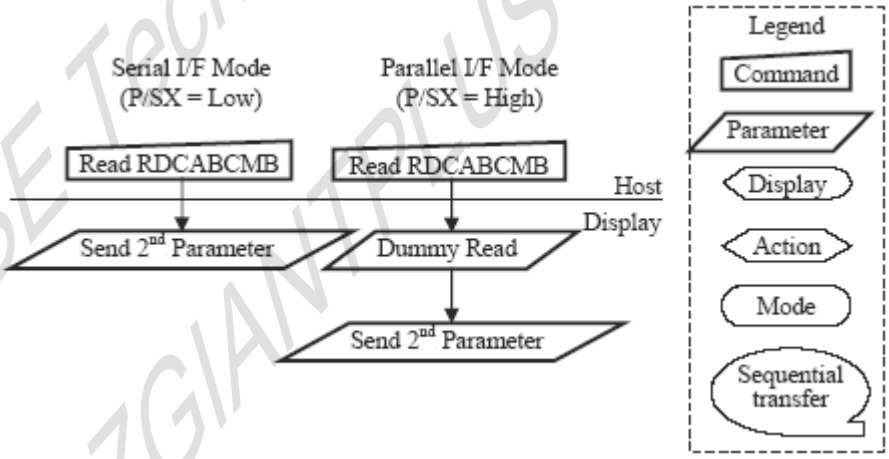
Register Availability

| Status | Availability |
|---|---|
| Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | $00_{HEX}$ |
| S/W Reset | $00_{HEX}$ |
| H/W Reset | $00_{HEX}$ |

Flow Chart



### 6.2.45. RDABCSDR (68h) : Read Automatic Brightness Control Self-Diagnostic Result

| 68H | RDABCSDR (Read Automatic Brightness Control Self-Diagnostic Result) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 68 |
| 1 st parameter | 1 | ↑ | 1 | xx | xx | xx | xx | xx | xx | Xx | xx | xx |
| 2 nd parameter | 1 | ↑ | 1 | D7 | D6 | 0 | 0 | 0 | 0 | 0 | 0 | xx |
| Description | This command indicates the status of the display self-diagnostic results for automatic brightness control after Sleep Out -command as described in the table below:<br>● Bit D7 – Register Loading Detection<br>See section “7.12.1 Register loading Detection”.<br>● Bit D6 – Functionality Detection<br>See section “7.12.2 Functionality Detection“.<br>● Bits D5, D4, D3, D2, D1 and D0 are for future use and are set to ‘0’. | | | | | | | | | | | |
| Restrictions | | | | | | | | | | | | |

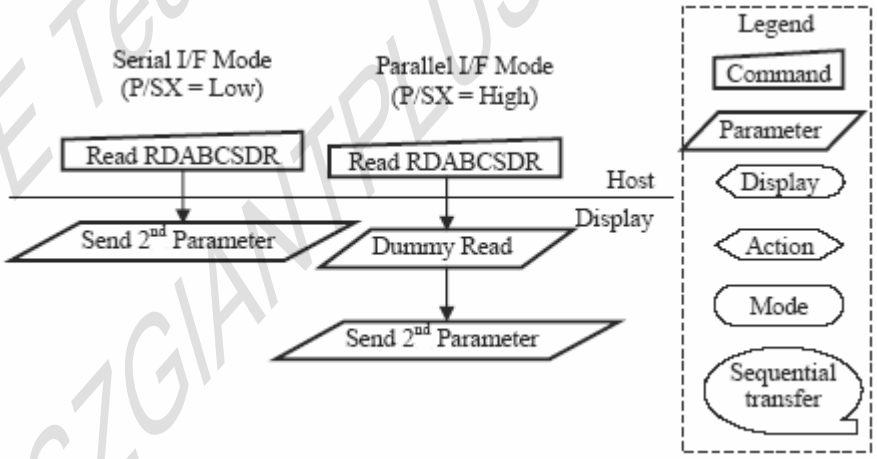
Register Availability

| Status | Availability |
|---|---|
| Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value |
|---|---|
| Power On Sequence | $00_{HEX}$ |
| S/W Reset | $00_{HEX}$ |
| H/W Reset | $00_{HEX}$ |

Flow Chart



### 6.3. Panel Command Description

#### 6.3.1. FRMCTR1 (B1h): Frame Rate Control

| B1H | FRMCTR1 (Frame Rate Control) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| FRMCTR1 | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | (B1h) |
| 1st Parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | FP [3] | FP [2] | FP [1] | FP [0] | - |
| 2nd Parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | BP [3] | BP [2] | BP [1] | BP [0] | - |
| 3rd Parameter | 1 | ↑ | 1 | - | 0 | 0 | RTN [5] | RTN [4] | RTN [3] | RTN [2] | RTN [1] | RTN [0] | - |

*NOTE: "-" Don't care*

**Description**

-Set the frame frequency of the full colors normal mode in MPU interface.

--The default vaule of BP0, FP0, and RTN0 can fit the frame frequency to be 60Hz ± 5%.

| FP [3:0] | Amount of Front Porch |
|---|---|
| 0 | 0 |
| 1 | 1 |
| 2 | 2 |
| 3 | 3 |
| 4 | 4 |
| … | … |
| B | 11 |
| C | 12 |
| D | 13 |
| E | 14 |
| F | 15 |

| BP [3:0] | Amount of Back Porch |
|---|---|
| 0 | 0 |
| 1 | 1 |
| 2 | 2 |
| 3 | 3 |
| 4 | 4 |
| … | … |
| D | 13 |
| E | 14 |
| F | 15 |

| RTN [3:0] | No. of clock in one line |
|---|---|
| 0 | 64 |
| 1 | 65 |
| 2 | 66 |
| 3 | 67 |
| 4 | 68 |
| … | … |
| 3D | 125 |
| 3E | 126 |
| 3F | 127 |

**Restriction**

-If this register not using the register need be reserved.

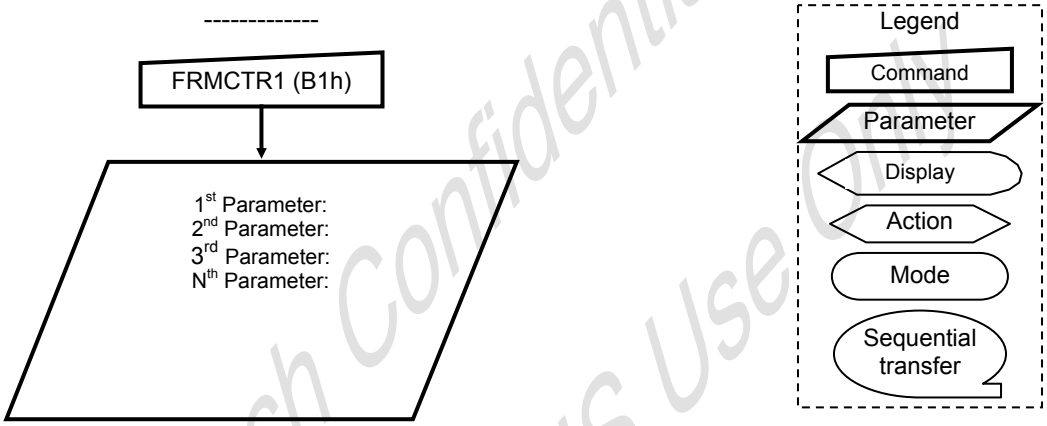
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | | |
|---|---|---|---|
| | FP | BP | RTN |
| Power On Sequence | 11d | 15d | 0d |
| S/W Reset | 11d | 15d | 0d |
| H/W Reset | 11d | 15d | 0d |

**Flow Chart**



### 6.3.2. INVCTR (B4h): Display Inversion Control

| B4H | INVCTR (Display Inversion Control) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| INVCTR | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | (B4h) |
| 1st Parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | NLA | NLB | NLC | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-Display Inversion mode control

-NLA: Inversion setting in full colors normal mode (Normal mode on)

| NLA | Inversion setting in full colours normal mode |
|---|---|
| **0** | **Line Inversion** |
| 1 | Frame Inversion |

-NLB: Inversion setting in Idle mode (Idle mode on)

| NLB | Inversion setting in Idle mode |
|---|---|
| 0 | Line Inversion |
| **1** | **Frame Inversion** |

-NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)

| NLC | Inversion setting in full colours partial mode |
|---|---|
| **0** | **Line Inversion** |
| 1 | Frame Inversion |

**Restriction**

-If this register not using the register need be reserved.

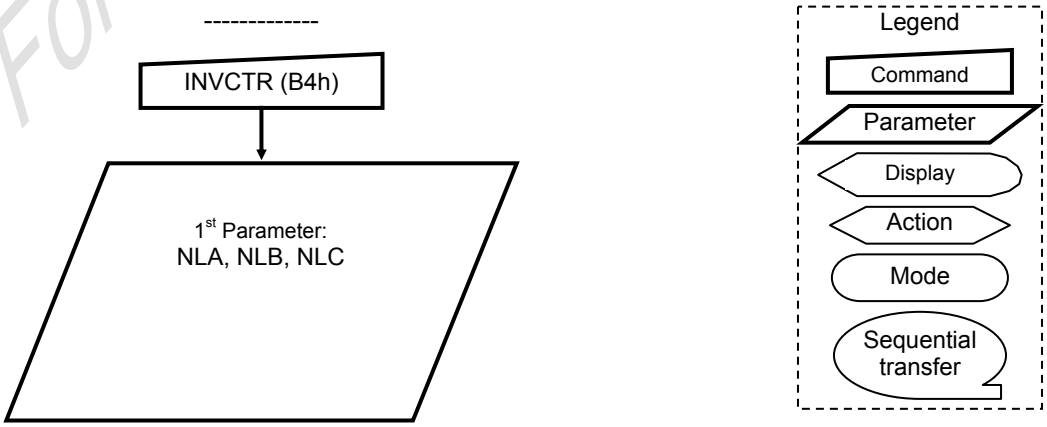
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | | | |
|---|---|---|---|---|
| | NLA | NLB | NLC | B4h |
| Power On Sequence | 0d | 1d | 0d | 02h |
| S/W Reset | 0d | 1d | 0d | 02h |
| H/W Reset | 0d | 1d | 0d | 02h |

**Flow Chart**



### 6.3.3. DISSET5 (B6h): Display Function set 5

| B6H | DISSET (Display Function set 5) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| DISSET5 | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | (B6h) |
| 1st Parameter | 1 | ↑ | 1 | - | 0 | 0 | NO1 | NO0 | SDT1 | STD0 | 0 | 0 | |
| 2nd Parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | PTG1 | PTG0 | PT1 | PT0 | |

*NOTE: "-" Don't care*

**Description**

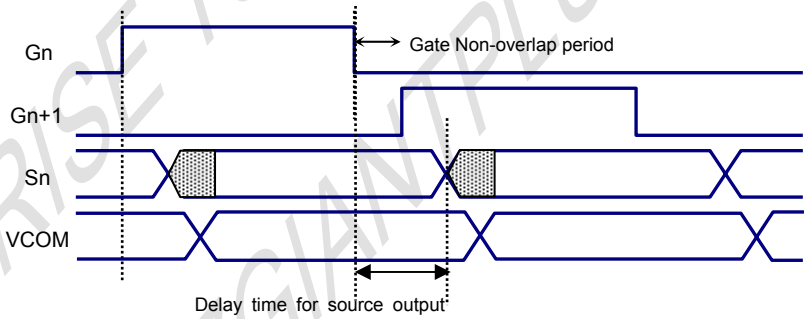
-1st parameter: Set output waveform relation.

-NO[1:0]: Set the amount of non-overlap of the gate output

| NO[1:0] | | Amount of non-overlap of the gate output |
|---|---|---|
| | | Refer the Internal oscillator |
| 00 | 0 | 16 clock cycle |
| 01 | 1 | 20 clock cycle |
| 10 | 2 | 24 clock cycle |
| 11 | 3 | 28 clock cycle |

-SDT[1:0]: Set delay amount from gate signal falling edge of the source output.

| SDT[1:0] | | Amount of non-overlap of the source output |
|---|---|---|
| | | Refer the Internal oscillator |
| 00 | 0 | 2 clock cycle |
| 01 | 1 | 4 clock cycle |
| 10 | 2 | 6 clock cycle |
| 11 | 3 | 8 clock cycle |




-2nd parameter: Set the output waveform in non-display area.

-PTG[1:0]: Determine gate output in a non-display area in the partial mode

| PTG[1:0] | | Gate output in a non-display area |
|---|---|---|
| 00 | 0 | Normal scan |
| 01 | 1 | Fix on VGL |
| 10 | 2 | Fix on VGL |
| 11 | 3 | Fix on VGL |

-PT[1:0]: Determine Source /VCOM output in a non-display area in the partial mode

| PT[1:0] | | Source output on non-display area | | VCOM output on non-display area | |
|---|---|---|---|---|---|
| | | Positive | Negative | Positive | Negative |
| 00 | 0 | V63 | V0 | VCOML | VCOMH |
| 01 | 1 | V0 | V63 | VCOML | VCOMH |
| 10 | 2 | VSSA | VSSA | VSSA | VSSA |
| 11 | 3 | Hi-z | Hi-z | VSSA | VSSA |

**Restriction**

-If this register not using the register need be reserved.

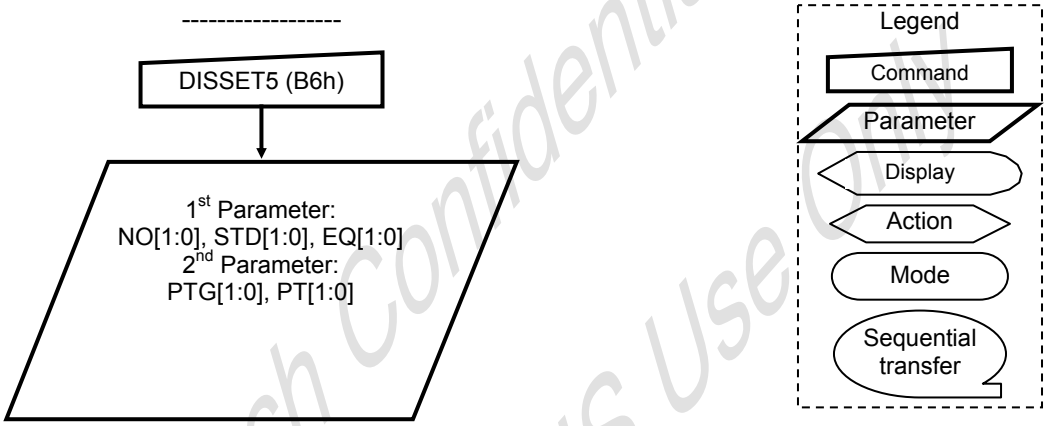
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | | | |
|---|---|---|---|---|
| | NO[1:0] | STD[1:0] | PTG[1:0] | PT[1:0] |
| Power On Sequence | 1d | 1d | 0d | 0d |
| S/W Reset | 1d | 1d | 0d | 0d |
| H/W Reset | 1d | 1d | 0d | 0d |

Flow Chart



### 6.3.4. FRADJ (BAh): Frame Rate ADJustment

| BAH | ENOM (BAh): Frame Rate ADJustment | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| FRADJ | 0 | ↑ | 1 | - | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | (BAh) |
| 1st Parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | FR3 | FR2 | FR1 | FR0 | |

*NOTE: "-" Don't care, can be set to VDDI or DGND level*

**Description**

This command can adjust Frame Rate.

-FR[3:0]: Determine Frame Rate.

| FR[1:0] | | Frame Frequency (Hz) | OSC Frequency |
|---|---|---|---|
| 0000 | 0 | 35 Hz | 772K Hz |
| 0001 | 1 | 40 Hz | 885K HZ |
| 0010 | 2 | 45 Hz | 996K HZ |
| 0011 | 3 | 50 Hz | 1107K Hz |
| 0100 | 4 | 42 Hz | 930K Hz |
| 0101 | 5 | 48 Hz | 1062K Hz |
| 0110 | 6 | 54 Hz | 1195K Hz |
| 0111 | 7 | 60 Hz | 1328K Hz |
| 1000 | 8 | 53 Hz | 1162K Hz |
| 1001 | 9 | 60 Hz | 1328K Hz |
| 1010 | 10 | 68 Hz | 1494K Hz |
| 1011 | 11 | 75 Hz | 1660K Hz |
| 1100 | 12 | 70 Hz | 1550K Hz |
| 1101 | 13 | 80 Hz | 1771K Hz |
| 1110 | 14 | 90 Hz | 1992K Hz |
| 1111 | 15 | 100 Hz | 2214K Hz |

**Restriction**

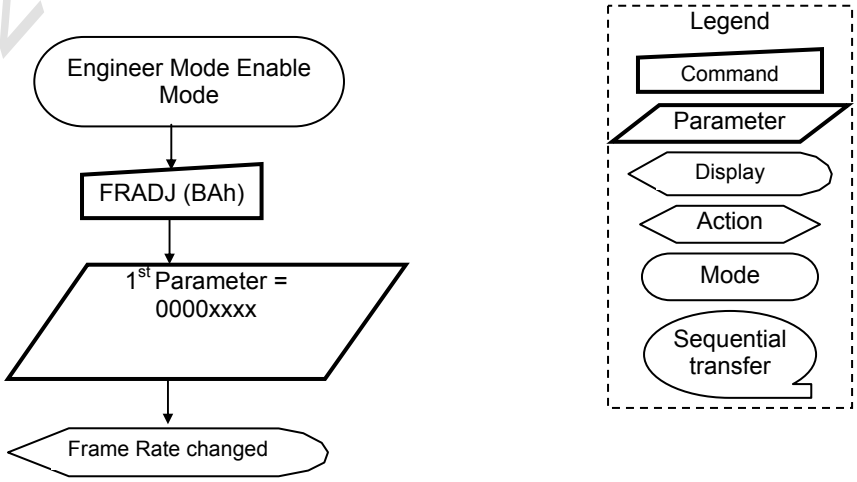
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out, Engineer Mode | Yes |
| Normal Mode On, Idle Mode On, Sleep Out, Engineer Mode | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out, Engineer Mode | Yes |
| Partial Mode On, Idle Mode On, Sleep Out, Engineer Mode | Yes |
| Sleep In | Yes |

**Default**

| Status | Parameter 1 default Value |
|---|---|
| Power On Sequence | 0000_0111 (07h) |
| S/W Reset | 0000_0111 (07h) |
| H/W Reset | 0000_0111 (07h) |

**Flow Chart**



### 6.3.5. PWCTR1 (C0h): Power Control 1

| C0H | PWCTR1 (Power Control 1) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| PWCTR1 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | (C0h) |
| 1st Parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | VRH4 | VRH3 | VRH2 | VRH1 | VRH0 | |
| 2nd Parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | VCI2 | VCI1 | VCI0 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-Set the GVDD and VCI1 voltage

| VRH[4:0] | | GVDD |
|---|---|---|
| Binary | HEX | Votage |
| 00000 | 00h | 3.00 V |
| 00001 | 01h | 3.10 V |
| 00010 | 02h | 3.20 V |
| 00011 | 03h | 3.30 V |
| 00100 | 04h | 3.40 V |
| 00101 | 05h | 3.50 V |
| 00110 | 06h | 3.60 V |
| 00111 | 07h | 3.70 V |
| 01000 | 08h | 3.80 V |
| 01001 | 09h | 3.90 V |
| 01010 | 0Ah | 3.95 V |
| 01011 | 0Bh | 4.00 V |
| 01100 | 0Ch | 4.05 V |
| 01101 | 0Dh | 4.10 V |
| 01110 | 0Eh | 4.15 V |
| 01111 | 0Fh | 4.20 V |
| 10000 | 10h | 4.25 V |
| 10001 | 11h | 4.30 V |
| 10010 | 12h | 4.35 V |
| 10011 | 13h | 4.40 V |
| 10100 | 14h | 4.45 V |
| 10101 | 15h | 4.50 V |
| 10110 | 16h | 4.55 V |
| 10111 | 17h | 4.60 V |
| 11000 | 18h | 4.65 V |
| 11001 | 19h | 4.70 V |
| 11010 | 1Ah | 4.75 V |
| 11011 | 1Bh | 4.80 V |
| 11100 | 1Ch | 4.85 V |
| 11101 | 1Dh | 4.90 V |
| 11110 | 1Eh | 4.95 V |
| 11111 | 1Fh | 5.00 V |

| VC[2:0] | | VCI1 |
|---|---|---|
| Binary | HEX | Votage |
| 000 | 0h | 2.5 V |
| 001 | 1h | 2.55 V |
| 010 | 2h | 2.60 V |
| 011 | 3h | 2.65 V |
| 100 | 4h | 2.70 V |
| 101 | 5h | 2.75 V |
| 110 | 6h | 2.80V |
| 111 | 7h | 2.90V |
| | | |

**Restriction**

-If this register not using the register need be reserved.

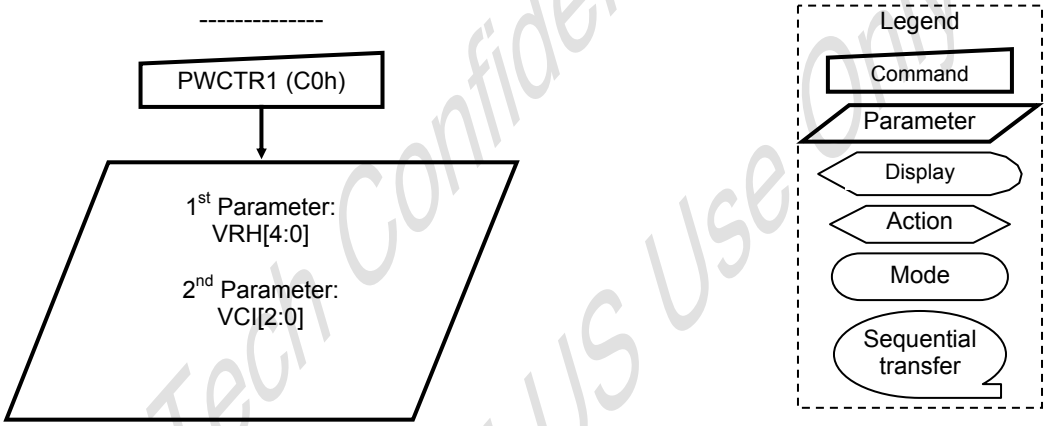
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | LCM = '00' TR LC type | | LCM = '01' TM LC type | | LCM = '10' LV LC type | | LCM = '11' MVA LC type | |
| | VRH [4:0] | VC [2:0] | VRH [4:0] | VC [2:0] | VRH [4:0] | VC [2:0] | VRH [4:0] | VC [2:0] |
| Power On Sequence | 16h | 3h | 16h | 3h | 16h | 3h | 16h | 3h |
| S/W Reset | 16h | 3h | 16h | 3h | 16h | 3h | 16h | 3h |
| H/W Reset | 16h | 3h | 16h | 3h | 16h | 3h | 16h | 3h |

**Flow Chart**



### 6.3.6. PWCTR3 (C2h): Power Control 3

| C2H | PWCTR3 (Power Control 3) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| PWCTR3 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | (C2h) |
| 1st Parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | AP2 | AP1 | AP0 | |

*NOTE: "-" Don't care*

**Description**

-Set the amount of current in Operational amplifier in normal mode/full colors.

-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the analog circuit.

| AP[2:0] | | Amount of Current in Operational Amplifier |
|---|---|---|
| 000 | 0 | Operation of the operational amplifier stops |
| 001 | 1 | Small |
| 010 | 2 | Medium Low |
| 011 | 3 | Medium |
| **100** | **4** | Medium High |
| 101 | 5 | Large |
| 110 | 6 | Reserved |
| 111 | 7 | Reserved |

**Restriction**

-If some parameter of the register not use the register need to be reserved.

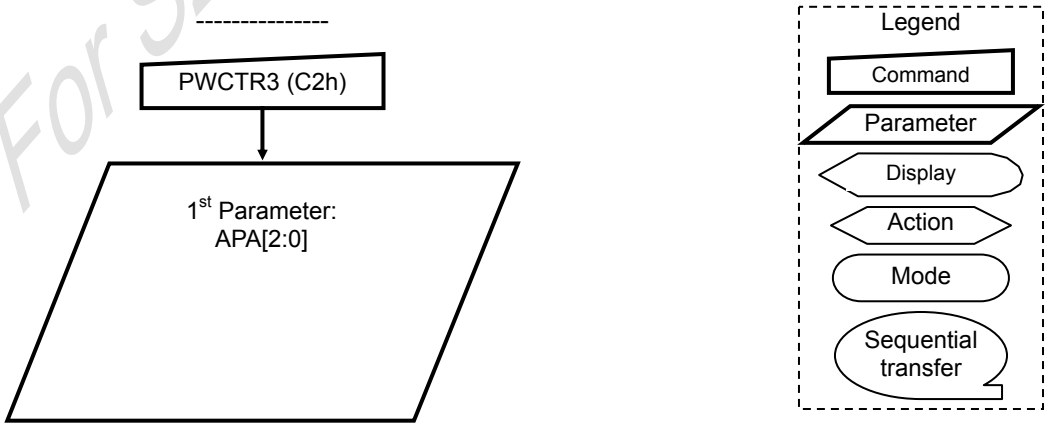
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| | AP[2:0] |
| Power On Sequence | 4d |
| S/W Reset | 4d |
| H/W Reset | 4d |

**Flow Chart**



### 6.3.7. PWCTR2 (C3h): Power Control 2

| C3H | PWCTR2 (Power Control 2) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| PWCTR2 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | (C3h) |
| 1st Parameter | 1 | ↑ | 1 | | 0 | 0 | 0 | 0 | 0 | BT2 | BT1 | BT0 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-Set the AVDD, VCL, VGH and VGL supply power level

| BT[2:0] | | AVDD | VCL | VGH | VGL |
|---|---|---|---|---|---|
| 000 | 0 | 2xVCI1 | -1xVCI1 | 6*VCI1 | -5*VCI1 |
| 001 | 1 | 2xVCI1 | -1xVCI1 | 6*VCI1 | -4*VCI1 |
| 010 | 2 | 2xVCI1 | -1xVCI1 | 6*VCI1 | -3*VCI1 |
| 011 | 3 | 2xVCI1 | -1xVCI1 | 5*VCI1 | -5*VCI1 |
| 100 | 4 | 2xVCI1 | -1xVCI1 | 5*VCI1 | -4*VCI1 |
| 101 | 5 | 2xVCI1 | -1xVCI1 | 5*VCI1 | -3*VCI1 |
| 110 | 6 | 2xVCI1 | -1xVCI1 | 4*VCI1 | -4*VCI1 |
| 111 | 7 | 2xVCI1 | -1xVCI1 | 4*VCI1 | -3*VCI1 |

**Restriction**

-If this register not using the register need be reserved.

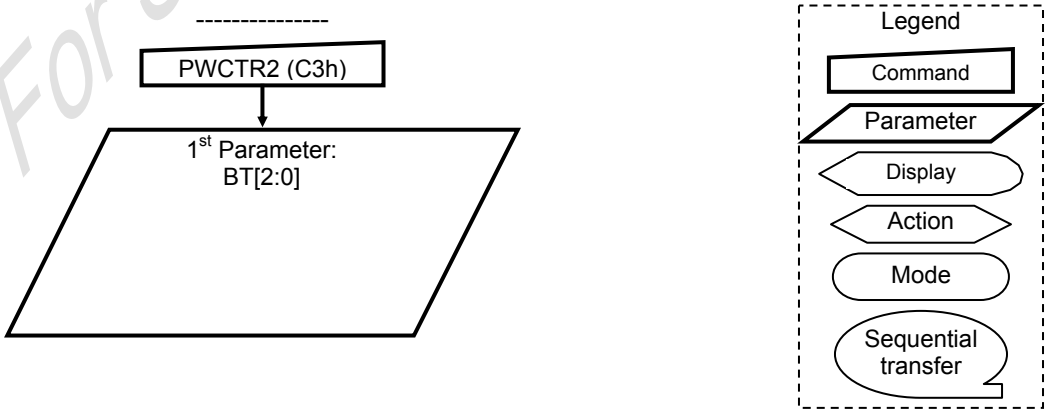
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| | BT[2:0] |
| Power On Sequence | 7d |
| S/W Reset | 7d |
| H/W Reset | 7d |

**Flow Chart**



### 6.3.8. PWCTR5 (C4h): Power Control 5

| C4H | PWCTR5 (Power Control 5) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| PWCTR5 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | (C4h) |
| 1st Parameter | 1 | ↑ | 1 | - | 0 | 0 | DC2[1] | DC2[0] | 0 | 0 | DC1[1] | DC1[0] | |

*NOTE: "-" Don't care*

**Description**

-Set the Booster circuit Step-up cycle

| DC1 [2:0] | | BCLK(Hz) |
|---|---|---|
| 00 | 1 line = 2BCLK | 41,400 |
| 01 | 1 line = 4BCLK | 82,800 |
| 10 | 1 line = 5BCLK | 165,600 |
| 11 | 1 line = 16BCLK | 331200 |

| DC2 [2:0] | | BCLK(Hz) |
|---|---|---|
| 00 | 1 line = 1BCLK | 20,700 |
| 01 | 1 line = 2BCLK | 41,400 |
| 10 | 1 line = 4BCLK | 82,800 |
| 11 | 1 line = 8BCLK | 165,600 |

*Note: BCLK is Clock frequency for Booster circuit*

**Restriction**

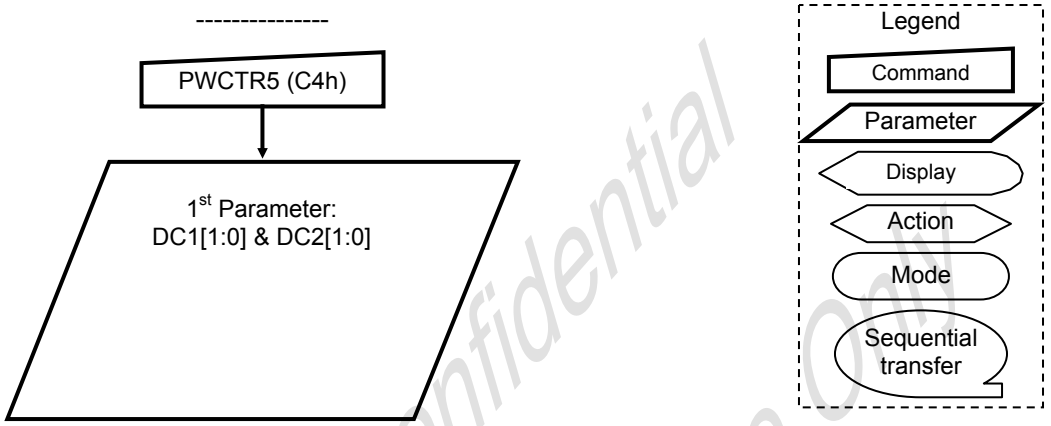
-If some parameters of the register not use the register need to be reserved.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | |
|---|---|---|
| | DC1 [1:0] | DC1 [1:0] |
| Power On Sequence | 0d | 0d |
| S/W Reset | 0d | 0d |
| H/W Reset | 0d | 0d |

| | |
|---|---|
| Flow Chart |  |

### 6.3.9. VMCTR1 (C5h): VCOM Control 1

| C5H | VMCTR1 (VCOM Control 1) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| VMCTR1 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | (C5h) |
| 1st Parameter | 1 | ↑ | 1 | - | nVM * | VMH6 | VMH5 | VMH 4 | VMH 3 | VMH 2 | VMH 1 | VMH 0 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-Set **VCOMH** Voltage

| VMH[6:0] | | VCOMH | VMH[6:0] | | VCOMH | VMH[6:0] | | VCOMH | VMH[6:0] | | VCOMH |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Binary | HEX | Votage | Binary | HEX | Votage | Binary | HEX | Votage | Binary | HEX | Votage |
| 0000000 | 00h | 2.500 V | 0100000 | 20h | 3.14 V | 1000000 | 40h | 3.78 V | 1100000 | 60h | 4.42 V |
| 0000001 | 01h | 2.52 V | 0100001 | 21h | 3.16 V | 1000001 | 41h | 3.80 V | 1100001 | 61h | 4.44 V |
| 0000010 | 02h | 2.54 V | 0100010 | 22h | 3.18 V | 1000010 | 42h | 3.82 V | 1100010 | 62h | 4.46 V |
| 0000011 | 03h | 2.56 V | 0100011 | 23h | 3.20 V | 1000011 | 43h | 3.84 V | 1100011 | 63h | 4.48 V |
| 0000100 | 04h | 2.58 V | 0100100 | 24h | 3.22 V | 1000100 | 44h | 3.86 V | 1100100 | 64h | 4.50 V |
| 0000101 | 05h | 2.60 V | 0100101 | 25h | 3.24 V | 1000101 | 45h | 3.88 V | 1100101 | 65h | 4.52 V |
| 0000110 | 06h | 2.62 V | 0100110 | 26h | 3.26 V | 1000110 | 46h | 3.90 V | 1100110 | 66h | 4.54 V |
| 0000111 | 07h | 2.64 V | 0100111 | 27h | 3.28 V | 1000111 | 47h | 3.92 V | 1100111 | 67h | 4.56 V |
| 0001000 | 08h | 2.66 V | 0101000 | 28h | 3.30 V | 1001000 | 48h | 3.94 V | 1101000 | 68h | 4.58 V |
| 0001001 | 09h | 2.68 V | 0101001 | 29h | 3.32 V | 1001001 | 49h | 3.96 V | 1101001 | 69h | 4.60 V |
| 0001010 | 0Ah | 2.7 V | 0101010 | 2Ah | 3.34 V | 1001010 | 4Ah | 3.98 V | 1101010 | 6Ah | 4.62 V |
| 0001011 | 0Bh | 2.72 V | 0101011 | 2Bh | 3.36 V | 1001011 | 4Bh | 4.00 V | 1101011 | 6Bh | 4.64 V |
| 0001100 | 0Ch | 2.74 V | 0101100 | 2Ch | 3.38 V | 1001100 | 4Ch | 4.02 V | 1101100 | 6Ch | 4.66 V |
| 0001101 | 0Dh | 2.76 V | 0101101 | 2Dh | 3.40 V | 1001101 | 4Dh | 4.04 V | 1101101 | 6Dh | 4.68 V |
| 0001110 | 0Eh | 2.78 V | 0101110 | 2Eh | 3.42 V | 1001110 | 4Eh | 4.06 V | 1101110 | 6Eh | 4.70 V |
| 0001111 | 0Fh | 2.80 V | 0101111 | 2Fh | 3.44 V | 1001111 | 4Fh | 4.08 V | 1101111 | 6Fh | 4.72 V |
| 0010000 | 10h | 2.82 V | 0110000 | 30h | 3.46 V | 1010000 | 50h | 4.10 V | 1110000 | 70h | 4.74 V |
| 0010001 | 11h | 2.84 V | 0110001 | 31h | 3.48 V | 1010001 | 51h | 4.12 V | 1110001 | 71h | 4.76 V |
| 0010010 | 12h | 2.86 V | 0110010 | 32h | 3.50 V | 1010010 | 52h | 4.14 V | 1110010 | 72h | 4.78 V |
| 0010011 | 13h | 2.88 V | 0110011 | 33h | 3.52 V | 1010011 | 53h | 4.16 V | 1110011 | 73h | 4.80 V |
| 0010100 | 14h | 2.90 V | 0110100 | 34h | 3.54 V | 1010100 | 54h | 4.18 V | 1110100 | 74h | 4.82 V |
| 0010101 | 15h | 2.92 V | 0110101 | 35h | 3.56 V | 1010101 | 55h | 4.20 V | 1110101 | 75h | 4.84 V |
| 0010110 | 16h | 2.94 V | 0110110 | 36h | 3.58 V | 1010110 | 56h | 4.22 V | 1110110 | 76h | 4.86 V |
| 0010111 | 17h | 2.96 V | 0110111 | 37h | 3.60 V | 1010111 | 57h | 4.24 V | 1110111 | 77h | 4.88 V |
| 0011000 | 18h | 2.98 V | 0111000 | 38h | 3.62 V | 1011000 | 58h | 4.26 V | 1111000 | 78h | 4.90 V |
| 0011001 | 19h | 3.00 V | 0111001 | 39h | 3.64 V | 1011001 | 59h | 4.28 V | 1111001 | 79h | 4.92 V |
| 0011010 | 1Ah | 3.02 V | 0111010 | 3Ah | 3.66 V | 1011010 | 5Ah | 4.30 V | 1111010 | 7Ah | 4.94 V |
| 0011011 | 1Bh | 3.04 V | 0111011 | 3Bh | 3.68 V | 1011011 | 5Bh | 4.32 V | 1111011 | 7Bh | 4.96 V |
| 0011100 | 1Ch | 3.06 V | 0111100 | 3Ch | 3.70 V | 1011100 | 5Ch | 4.34 V | 1111100 | 7Ch | 4.98 V |
| 0011101 | 1Dh | 3.08 V | 0111101 | 3Dh | 3.72 V | 1011101 | 5Dh | 4.36 V | 1111101 | 7Dh | 5.00 V |
| 0011110 | 1Eh | 3.10 V | 0111110 | 3Eh | 3.74 V | 1011110 | 5Eh | 4.38 V | 1111110 | 7Eh | 5.02 V |
| 0011111 | 1Fh | 3.12 V | 0111111 | 3Fh | 3.76 V | 1011111 | 5Fh | 4.40 V | 1111111 | 7Fh | 5.04 V |

-Select the VCOMH value

| nVM * | VCOMH value |
|---|---|
| 0 | VCOMH value is from NV memory |
| 1 | VCOMH value is from the VCOMH[6:0] setting |

-The nVM need be used in 1st parameter of VMCTR1 (C5h)
- When nVM=0, the value of VMH[6:0] is from NV memory. So it must program the NV memory first.
- When nVM=1, the vaule of VMH[6:0] is from $C5 register. It can fine-tune the display performance to the best quality by setting this register, and program this optium value to NV memory.

**Restriction**

-If this register not using the register need be reserved.

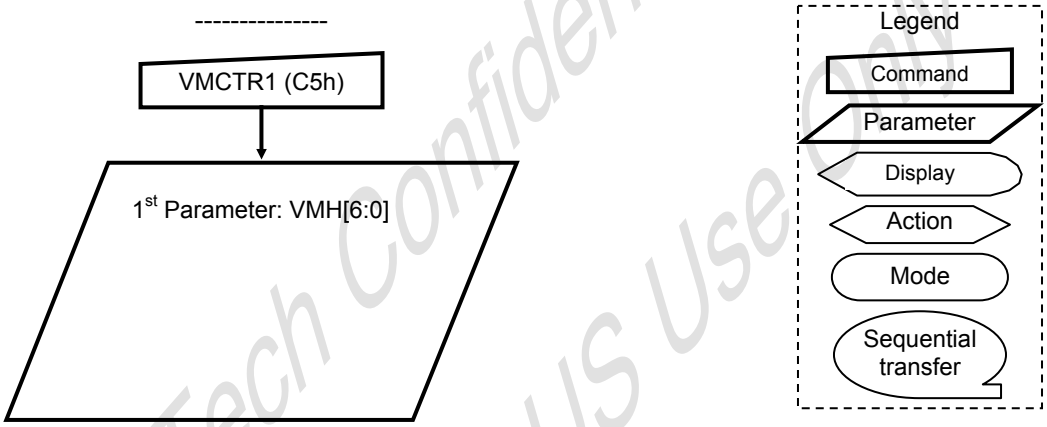
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default

| Status | Default Value | | | | |
|---|---|---|---|---|---|
| | nVM | LCM = '00' TR LC Type | LCM = '01' TM LC type | LCM = '10' LV LC type | LCM = '11' MVA LC type |
| | | VMH[6:0] | VMH[6:0] | VMH[6:0] | VMH[6:0] |
| Power On Sequence | 0d | 40h | 6Eh | 45h | 5FH |
| S/W Reset | 0d | 40h | 6Eh | 45h | 5FH |
| H/W Reset | 0d | 40h | 6Eh | 45h | 5FH |

Flow Chart



### 6.3.10. VMCTR2 (C6h): VCOM Control 2

| C6H | VMCTR2 (VCOM Control 2) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| VMCTR2 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | (C6h) |
| 1st Parameter | 1 | ↑ | 1 | - | 0 | VMA6 | VMA5 | VMA4 | VMA3 | VMA2 | VMA1 | VMA0 | |

*NOTE: "-" Don't care, can be set to VDDIO or VSS level*

**Description**

-Set **VCOMAC** Voltage

| VMA[6:0] | | VCOMAC | VMA[6:0] | | VCOMAC | VMA[6:0] | | VCOMAC | VMA[6:0] | | VCOMAC |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Binary | HEX | Votage | Binary | HEX | Votage | Binary | HEX | Votage | Binary | HEX | Votage |
| 0000000 | 00h | 3.00 V | 0100000 | 20h | 4.28 V | 1000000 | 40h | 5.56 V | 1100000 | 60h | 6.00 V |
| 0000001 | 01h | 3.04 V | 0100001 | 21h | 4.32 V | 1000001 | 41h | 5.60 V | 1100001 | 61h | 6.00 V |
| 0000010 | 02h | 3.08 V | 0100010 | 22h | 4.36 V | 1000010 | 42h | 5.64 V | 1100010 | 62h | 6.00 V |
| 0000011 | 03h | 3.12 V | 0100011 | 23h | 4.40 V | 1000011 | 43h | 5.68 V | 1100011 | 63h | 6.00 V |
| 0000100 | 04h | 3.16 V | 0100100 | 24h | 4.44 V | 1000100 | 44h | 5.72 V | 1100100 | 64h | 6.00 V |
| 0000101 | 05h | 3.20 V | 0100101 | 25h | 4.48 V | 1000101 | 45h | 5.76 V | 1100101 | 65h | 6.00 V |
| 0000110 | 06h | 3.24 V | 0100110 | 26h | 4.52 V | 1000110 | 46h | 5.80 V | 1100110 | 66h | 6.00 V |
| 0000111 | 07h | 3.28 V | 0100111 | 27h | 4.56 V | 1000111 | 47h | 5.84 V | 1100111 | 67h | 6.00 V |
| 0001000 | 08h | 3.32 V | 0101000 | 28h | 4.60 V | 1001000 | 48h | 5.88 V | 1101000 | 68h | 6.00 V |
| 0001001 | 09h | 3.36 V | 0101001 | 29h | 4.64 V | 1001001 | 49h | 5.92 V | 1101001 | 69h | 6.00 V |
| 0001010 | 0Ah | 3.40 V | 0101010 | 2Ah | 4.68 V | 1001010 | 4Ah | 5.96 V | 1101010 | 6Ah | 6.00 V |
| 0001011 | 0Bh | 3.44 V | 0101011 | 2Bh | 4.72 V | 1001011 | 4Bh | 6.00 V | 1101011 | 6Bh | 6.00 V |
| 0001100 | 0Ch | 3.48 V | 0101100 | 2Ch | 4.76 V | 1001100 | 4Ch | 6.00 V | 1101100 | 6Ch | 6.00 V |
| 0001101 | 0Dh | 3.52 V | 0101101 | 2Dh | 4.80 V | 1001101 | 4Dh | 6.00 V | 1101101 | 6Dh | 6.00 V |
| 0001110 | 0Eh | 3.56 V | 0101110 | 2Eh | 4.84 V | 1001110 | 4Eh | 6.00 V | 1101110 | 6Eh | 6.00 V |
| 0001111 | 0Fh | 3.60 V | 0101111 | 2Fh | 4.88 V | 1001111 | 4Fh | 6.00 V | 1101111 | 6Fh | 6.00 V |
| 0010000 | 10h | 3.64 V | 0110000 | 30h | 4.92 V | 1010000 | 50h | 6.00 V | 1110000 | 70h | 6.00 V |
| 0010001 | 11h | 3.68 V | 0110001 | 31h | 4.96 V | 1010001 | 51h | 6.00 V | 1110001 | 71h | 6.00 V |
| 0010010 | 12h | 3.72 V | 0110010 | 32h | 5.00 V | 1010010 | 52h | 6.00 V | 1110010 | 72h | 6.00 V |
| 0010011 | 13h | 3.76 V | 0110011 | 33h | 5.04 V | 1010011 | 53h | 6.00 V | 1110011 | 73h | 6.00 V |
| 0010100 | 14h | 3.80 V | 0110100 | 34h | 5.08 V | 1010100 | 54h | 6.00 V | 1110100 | 74h | 6.00 V |
| 0010101 | 15h | 3.84 V | 0110101 | 35h | 5.12 V | 1010101 | 55h | 6.00 V | 1110101 | 75h | 6.00 V |
| 0010110 | 16h | 3.88 V | 0110110 | 36h | 5.16 V | 1010110 | 56h | 6.00 V | 1110110 | 76h | 6.00 V |
| 0010111 | 17h | 3.92 V | 0110111 | 37h | 5.20 V | 1010111 | 57h | 6.00 V | 1110111 | 77h | 6.00 V |
| 0011000 | 18h | 3.96 V | 0111000 | 38h | 5.24 V | 1011000 | 58h | 6.00 V | 1111000 | 78h | 6.00 V |
| 0011001 | 19h | 4.00 V | 0111001 | 39h | 5.28 V | 1011001 | 59h | 6.00 V | 1111001 | 79h | 6.00 V |
| 0011010 | 1Ah | 4.04 V | 0111010 | 3Ah | 5.32 V | 1011010 | 5Ah | 6.00 V | 1111010 | 7Ah | 6.00 V |
| 0011011 | 1Bh | 4.08 V | 0111011 | 3Bh | 5.36 V | 1011011 | 5Bh | 6.00 V | 1111011 | 7Bh | 6.00 V |
| 0011100 | 1Ch | 4.12 V | 0111100 | 3Ch | 5.40 V | 1011100 | 5Ch | 6.00 V | 1111100 | 7Ch | 6.00 V |
| 0011101 | 1Dh | 4.16 V | 0111101 | 3Dh | 5.44 V | 1011101 | 5Dh | 6.00 V | 1111101 | 7Dh | 6.00 V |
| 0011110 | 1Eh | 4.20 V | 0111110 | 3Eh | 5.48 V | 1011110 | 5Eh | 6.00 V | 1111110 | 7Eh | 6.00 V |
| 0011111 | 1Fh | 4.24 V | 0111111 | 3Fh | 5.52 V | 1011111 | 5Fh | 6.00 V | 1111111 | 7Fh | 6.00 V |

**Restriction**

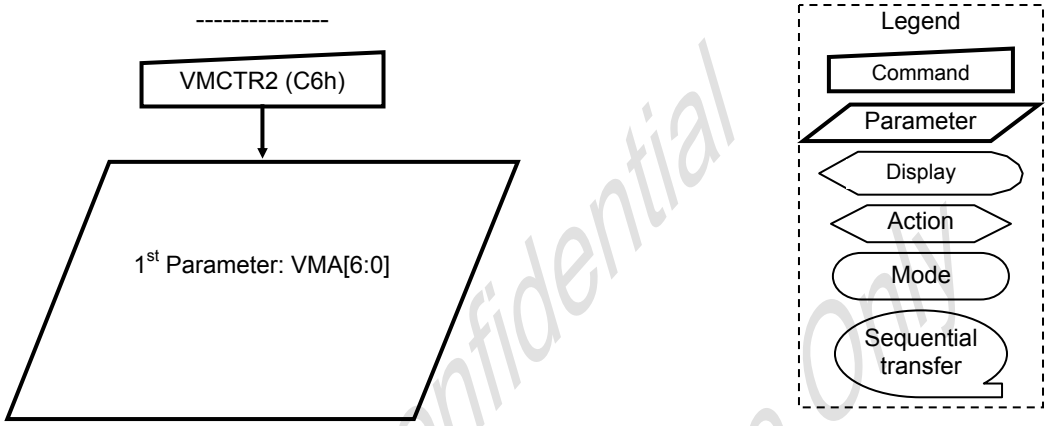
-If this register not use the register need be reserved.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

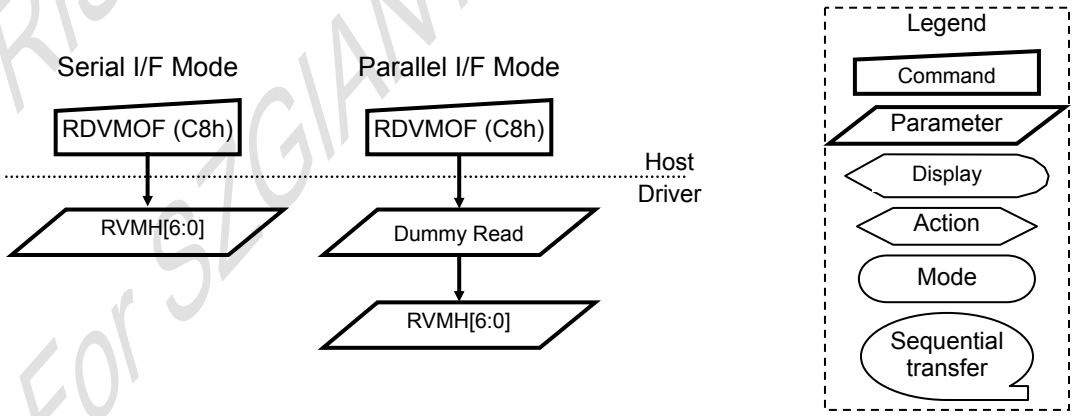
| Status | Default Value | | | |
|---|---|---|---|---|
| | LCM = '00' TR LC Type | LCM = '01' TM LC Type | LCM = '10' LV LC Type | LCM = '11' MVA LC type |
| | VMA[6:0] | VMA[6:0] | VMA[6:0] | VMA[6:0] |
| Power On Sequence | 30h | 40h | 27h | 28h |
| S/W Reset | 30h | 40h | 27h | 28h |
| H/W Reset | 30h | 40h | 27h | 28h |

| | |
|---|---|
| Flow Chart |  |

### 6.3.11. RDVMH (C8h): Read the VCOMH Value NV memory

| C8H | RDVMH (Read the VCOMH Value NV memory) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| RDVMOF | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | (C8h) |
| 1st Parameter | 0 | **1** | ↑ | - | - | - | - | - | - | - | - | - | - |
| 2nd Parameter | 1 | **1** | ↑ | - | nVM | RVMH6 | RVMH5 | RVMH4 | RVMH3 | RVMH2 | RVMH1 | RVMH0 | - |

*NOTE: "-" Don't care*

| | |
|---|---|
| Description | -Read the VCOMH value from NV memory<br>-The 1st parameter is dummy data.<br>-The 2nd parameter is RVMH[6:0] value from NV memory or default value. |
| Restriction | -If this register not use the register need be reserved. |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out: Yes<br>Normal Mode On, Idle Mode On, Sleep Out: Yes<br>Partial Mode On, Idle Mode Off, Sleep Out: Yes<br>Partial Mode On, Idle Mode On, Sleep Out: Yes<br>Sleep In: Yes |
| Default | Status / Default Value-<br>Power On Sequence: -<br>S/W Reset: -<br>H/W Reset: - |
| Flow Chart |  |



### 6.3.12. PWCTR6 (CBh): Power Control 6

| C2H | PWCTR6 (Power Control 6) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| PWCTR3 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | (CBh) |
| 1st Parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | GP2 | GP1 | GP0 | |

*NOTE: "-" Don't care*

| | |
|---|---|
| Description | -Set the amount of current in Operational amplifier in normal mode/full colors.<br>-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the Gamma |

| GP[2:0] | | Amount of Current in Operational Amplifier |
|---|---|---|
| 000 | 0 | Operation of the operational amplifier stops |
| 001 | 1 | Small |
| 010 | 2 | Medium Low |
| 011 | 3 | Medium |
| 100 | 4 | Medium High |
| 101 | 5 | Large |
| 110 | 6 | Reserved |
| 111 | 7 | Reserved |

Restriction: -If some parameter of the register not use the register need to be reserved.

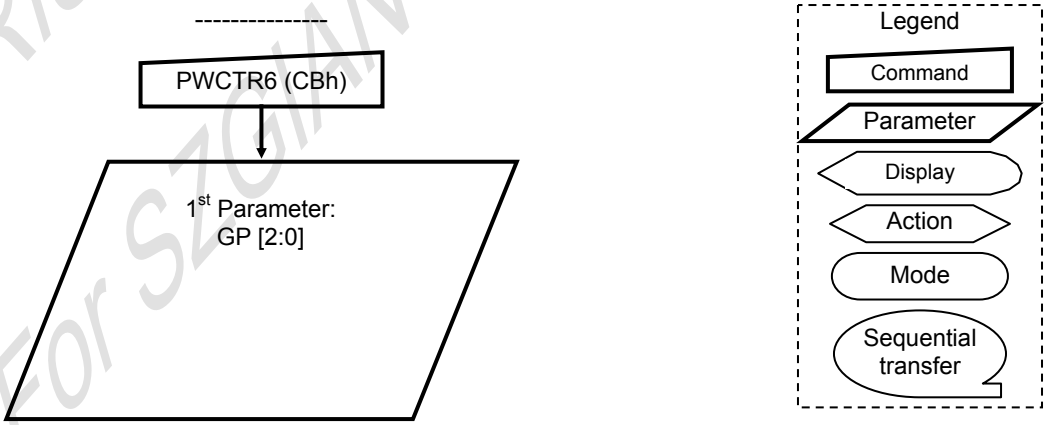
Register Availability:

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Default:

| Status | Default Value |
|---|---|
| | GP[2:0] |
| Power On Sequence | 4d |
| S/W Reset | 4d |
| H/W Reset | 4d |

Flow Chart:






### 6.3.13. PWCTR7 (CCh): Power Control 7

| C2H | PWCTR7 (Power Control 7) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| PWCTR3 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | (CCh) |
| 1st Parameter | 1 | ↑ | 1 | - | 0 | 0 | 0 | 0 | 0 | SP2 | SP1 | SP0 | |

*NOTE: "-" Don't care*

**Description**

-Set the amount of current in Operational amplifier in normal mode/full colors.

-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver

| SP[2:0] | | Amount of Current in Operational Amplifier |
|---|---|---|
| 000 | 0 | Operation of the operational amplifier stops |
| 001 | 1 | Small |
| 010 | 2 | Medium Low |
| 011 | 3 | Medium |
| **100** | **4** | Medium High |
| 101 | 5 | Large |
| 110 | 6 | Reserved |
| 111 | 7 | Reserved |

**Restriction**

-If some parameter of the register not use the register need to be reserved.

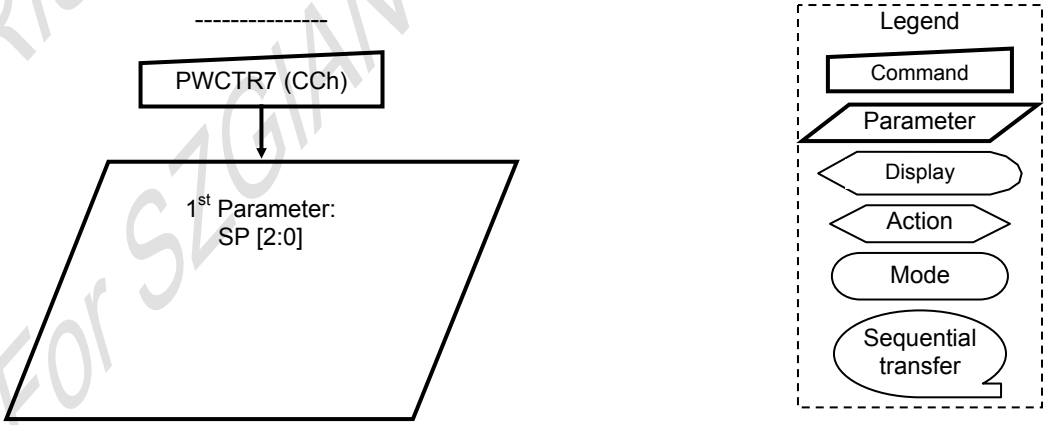
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| | SP[2:0] |
| Power On Sequence | 4d |
| S/W Reset | 4d |
| H/W Reset | 4d |

**Flow Chart**



### 6.3.14. WRID1 (D0h): Write ID1 Value

| D1H | WRID2 (Write ID2 Value) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| WRID2 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | (D0h) |
| 1st Parameter | 1 | ↑ | 1 | - | 1 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | - |

*NOTE: "-" Don't care*

**Description**

-Write 7-bits data of LCD module version to save it to NV memory.

-The 1st parameter ID1[6:0] is LCD Module version ID.

**Restriction**

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Not Fixed |
| S/W Reset | Not Fixed |
| H/W Reset | Not Fixed |

**Flow Chart**

### 6.3.15. WRID2 (D1h): Write ID2 Value

| D1H | WRID2 (Write ID2 Value) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| WRID2 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | (D1h) |
| 1st Parameter | 1 | ↑ | 1 | - | 1 | ID26 | ID25 | ID24 | ID23 | ID22 | ID21 | ID20 | - |

*NOTE: "-" Don't care*

**Description**

-Write 7-bits data of LCD module version to save it to NV memory.

-The 1st parameter ID2[6:0] is LCD Module version ID.

**Restriction**

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value |
|---|---|
| Power On Sequence | Not Fixed |
| S/W Reset | Not Fixed |
| H/W Reset | Not Fixed |

**Flow Chart**

### 6.3.16. WRID3 (D2h): Write ID3 Value

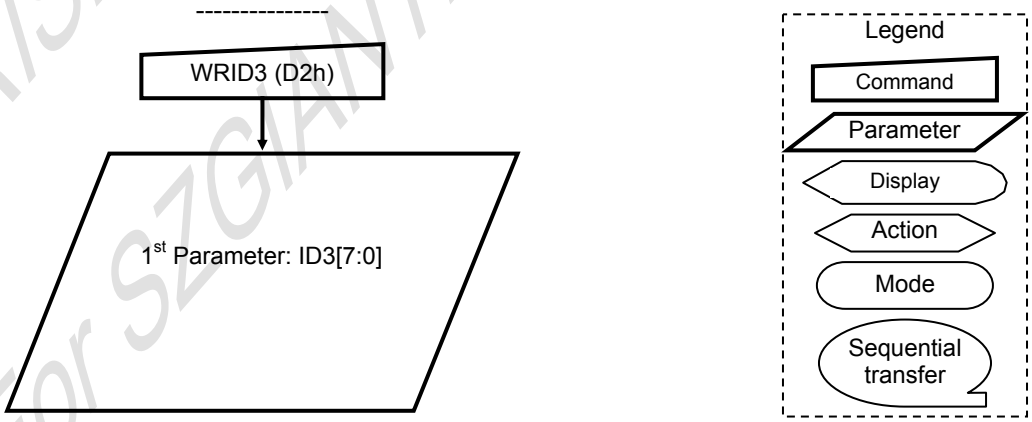
| D2H | WRID3 (Write ID3 Value) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| WRID3 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | (D2h) |
| 1st Parameter | 1 | ↑ | 1 | - | ID37 | ID36 | ID35 | ID34 | ID33 | ID32 | ID31 | ID30 | |

*NOTE: "-" Don't care*

| | |
|---|---|
| Description | -Write 8-bits data of project code module to save it to NV memory.<br>-The 1st parameter ID3[7:0] is product project ID. |
| Restriction | |
| Register Availability | |
| Default | |
| Flow Chart | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

| Status | Default Value |
|---|---|
| Power On Sequence | 00h |
| S/W Reset | 00h |
| H/W Reset | 00h |



### 6.3.17. RDID4 (D3h): Read the ID4 value

| D3H | RDID4 (Read the ID4 value) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| RDID4 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | (D3h) |
| 1st Parameter | 1 | 1 | ↑ | - | - | - | - | - | - | - | - | - | |
| 2nd Parameter | 1 | 1 | ↑ | - | ID417 | ID416 | ID415 | ID414 | ID413 | ID412 | ID411 | ID410 | - |
| 3rd Parameter | 1 | 1 | ↑ | - | ID427 | ID426 | ID425 | ID424 | ID423 | ID422 | ID421 | ID420 | - |
| 4th Parameter | 1 | 1 | ↑ | - | ID437 | ID436 | ID435 | ID434 | ID433 | ID432 | ID431 | ID430 | - |
| 5th Parameter | 1 | 1 | ↑ | - | ID447 | ID446 | ID445 | ID444 | ID443 | ID442 | ID441 | ID440 | - |

*NOTE: "-" Don't care*

**Description**

-Read the Driver IC information from mask value.
-The 1st parameter is dummy data.
-The 2nd parameter ID41[7:0] is Driver IC ID code.
-ID41[7:0] is 06H.
-The 3rd parameter ID42[7:0] is Driver IC Part number ID. It is 14H.
-The 4th & 5th parameter ID43[7:0] & ID44[7:0] are Driver IC version ID.

**Restriction**

-

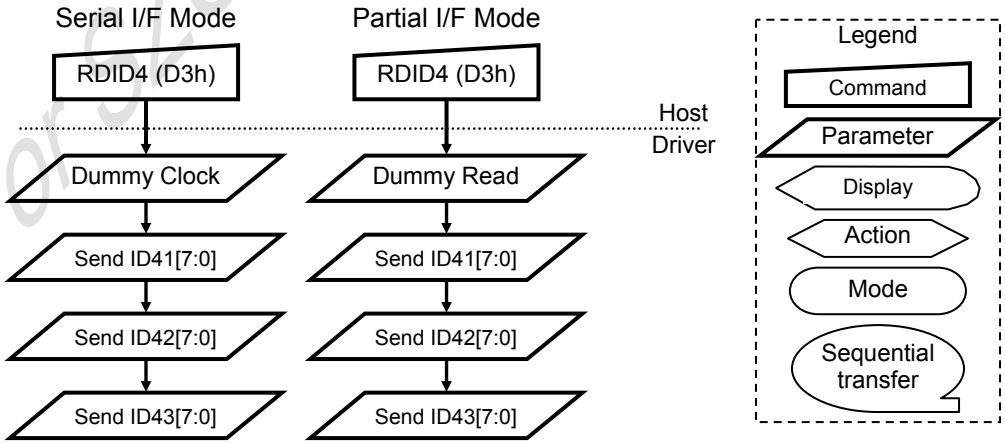
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value- | | | |
|---|---|---|---|---|
| | ID41[7:0] | ID42[7:0] | ID43[7:0] | ID44[7:0] |
| Power On Sequence | 06H | 06H | 01H | 00H |
| S/W Reset | 06H | 06H | 01H | 00H |
| H/W Reset | 06H | 06H | 01H | 00H |

**Flow Chart**



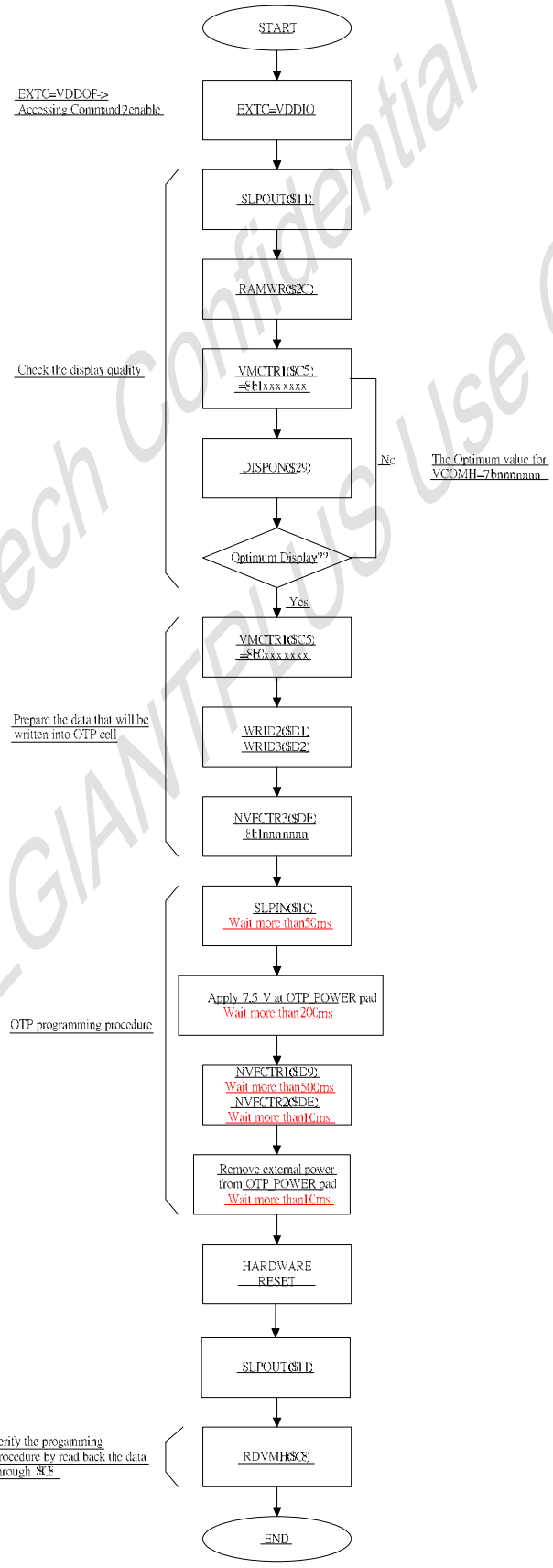
### 6.3.18. NVFCTR1 (D9h): NV Memory Function Controller 1

| D9H | NVFCTR1 (NV Memory Function Controller 1) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| NVFCTR1 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | (D9h) |

*NOTE: "-" Don't care1*

Description

- Write WVMH[6:0] for VCOMH voltage to $D9 when the value is considered as the optimum for display quality.
- The endurence for OTM3206A NV memory is 4 times for ID2, ID3, and VCOMH.

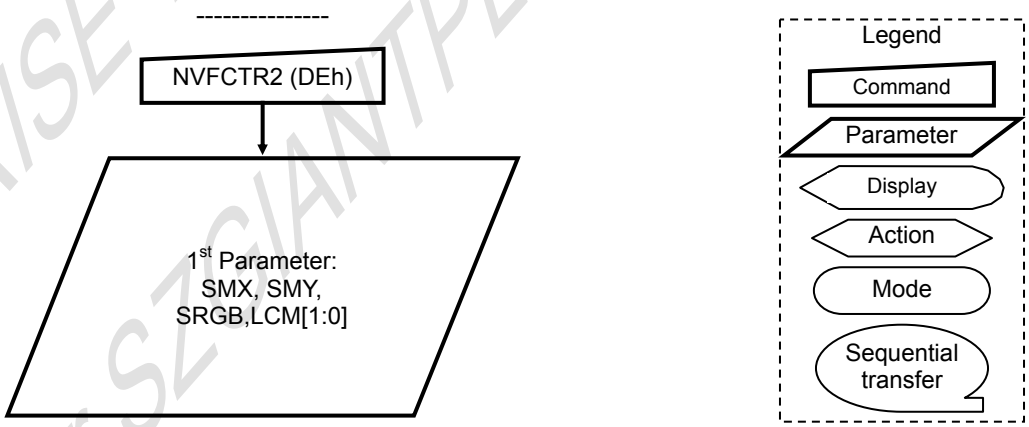


<table>
<tr><td>Restriction</td><td>The endurence of ID2, ID3, and VMH is 4 times.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Not Fixed</td></tr>
<tr><td>S/W Reset</td><td>Not Fixed</td></tr>
<tr><td>H/W Reset</td><td>Not Fixed</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>
---------- <br>
NVFCTR1 (D9h) <br>
Legend <br>
Command <br>
Parameter <br>
Display <br>
Action <br>
Mode <br>
Sequential transfer
</td></tr>
</table>

### 6.3.19. NVFCTR2 (DEh): NV Memory Function Controller 2

| DEH | NVFCTR2 (NV Memory Function Controller 2) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| NVFCTR2 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | (DEh) |
| 1st Parameter | 1 | ↑ | 1 | - | 1 | SMY | SMX | SRGB | 0 | 0 | LCM1 | LCM0 | - |

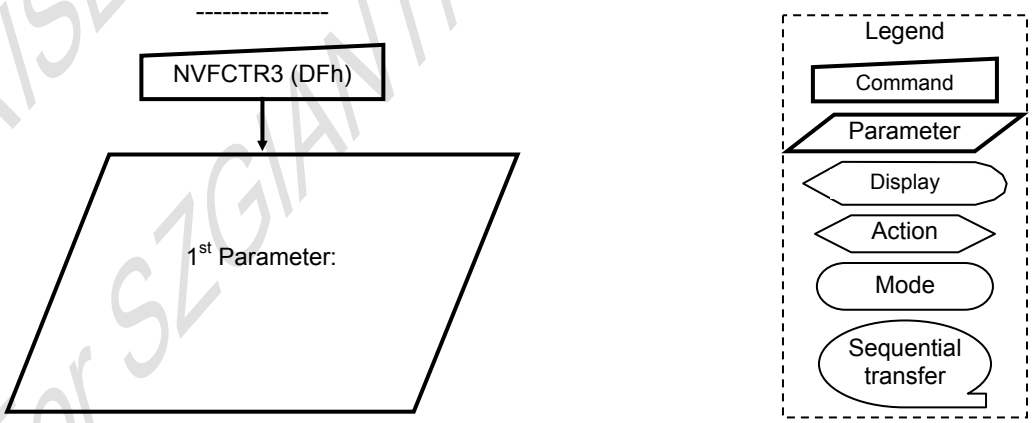
*NOTE: "-" Don't care*

| | |
|---|---|
| Description | **- Please refer to $D9 for details.**<br>-Write LCM[1:0], SRGB, SMX and SMY to NV memory.<br>- SMY is Gate driver output direction selection<br>- SMX is Source driver output direction selection<br>- SRGB is RGB arrangement selection:<br>- LCM[1:0] is Liquid Crystal Type selection. |
| Restriction | |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out: Yes<br>Normal Mode On, Idle Mode On, Sleep Out: Yes<br>Partial Mode On, Idle Mode Off, Sleep Out: Yes<br>Partial Mode On, Idle Mode On, Sleep Out: Yes<br>Sleep In: Yes |
| Flow Chart |  |

### 6.3.20. NVFCTR3 (DFh): NV Memory Function Controller 3

| DEH | NVFCTR3 (NV Memory Function Controller 3) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| NVFCTR3 | 0 | ↑ | 1 | - | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | (DFh) |
| 1st Parameter | 1 | ↑ | 1 | - | 1 | VMH6 | VMH5 | VMH4 | VMH3 | VMH2 | VMH1 | VMH0 | - |
| 2st Parameter | 1 | ↑ | 1 | | - | VMA6- | VMA5 | VMA4 | VMA3 | VMA2 | VMA1 | VMA0 | |

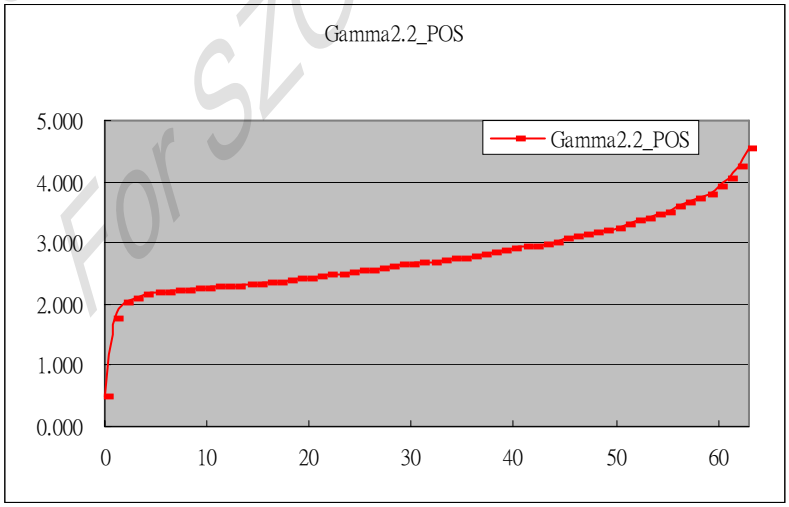
*NOTE: "-" Don't care*

| | |
|---|---|
| Description | **- Please refer to $D9 for details.** |
| Restriction | |
| Register Availability | Status: Availability<br>Normal Mode On, Idle Mode Off, Sleep Out: Yes<br>Normal Mode On, Idle Mode On, Sleep Out: Yes<br>Partial Mode On, Idle Mode Off, Sleep Out: Yes<br>Partial Mode On, Idle Mode On, Sleep Out: Yes<br>Sleep In: Yes |
| Default | Status: Default Value<br>Power On Sequence: Not Fixed<br>S/W Reset: Not Fixed<br>H/W Reset: Not Fixed |
| Flow Chart |  |

### 6.3.21. GMCTRP(E0h): Gamma Correction Characteristics Setting

| E0H | GMCTRP1 (Gamma '+'polarity Correction Characteristics Setting) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| GMCTRP1 | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | (E0h) |
| 1st Parameter | 1 | ↑ | 1 | - | - | - | PVR1 V0[5]- | PVR1 V0[4] | PVR1 V0[3] | PVR1 V0[2] | PVR1 V0[1] | PVR1 V0[0] | |
| 2nd Parameter | 1 | ↑ | 1 | - | - | - | PVR1 V1[5] | PVR1 V1[4] | PVR1 V1[3] | PVR1 V1[2] | PVR1 V1[1] | PVR1 V1[0] | |
| 3rd Parameter | 1 | ↑ | 1 | - | - | - | PVR1 V2[5] | PVR1 V2[4] | PVR1 V2[3] | PVR1 V2[2] | PVR1 V2[1] | PVR1 V2[0] | |
| 4th Parameter | 1 | ↑ | 1 | - | - | - | PVR1 V61[5] | PVR1 V61[4] | PVR1 V61[3] | PVR1 V61[2] | PVR1 V61[1] | PVR1 V61[0] | |
| 5th Parameter | 1 | ↑ | 1 | - | - | - | PVR1 V62[5] | PVR1 V62[4] | PVR1 V62[3] | PVR1 V62[2] | PVR1 V62[1] | PVR1 V62[0] | |
| 6th Parameter | 1 | ↑ | 1 | - | - | - | PVR1 V63[5]- | PVR1 V63[4] | PVR1 V63[3] | PVR1 V63[2] | PVR1 V63[1] | PVR1 V63[0] | |
| 7th Parameter | 1 | ↑ | 1 | - | - | - | PVR2 V13[5] | PVR2 V13[4] | PVR2 V13[3] | PVR2 V13[2] | PVR2 V13[1] | PVR2 V13[0] | |
| 8th Parameter | 1 | ↑ | 1 | - | - | - | PVR2 V50[5] | PVR2 V50[4] | PVR2 V50[3] | PVR2 V50[2] | PVR2 V50[1] | PVR2 V50[0] | |
| 9th Parameter | 1 | ↑ | 1 | - | - | - | - | - | PVR3 V4[3] | PVR3 V4[2] | PVR3 V4[1] | PVR3 V4[0] | |
| 10th Parameter | 1 | ↑ | 1 | - | - | - | - | - | PVR3 V8[3] | PVR3 V8[2] | PVR3 V8[1] | PVR3 V8[0] | |
| 11th Parameter | 1 | ↑ | 1 | - | - | - | - | - | PVR3 V20[3] | PVR3 V20[2] | PVR3 V20[1] | PVR3 V20[0] | |
| 12th Parameter | 1 | ↑ | 1 | - | - | - | - | - | PVR3 V27[3] | PVR3 V27[2] | PVR3 V27[1] | PVR3 V27[0] | |
| 13th Parameter | 1 | ↑ | 1 | - | - | - | - | - | PVR3 V36[3] | PVR3 V36[2] | PVR3 V36[1] | PVR3 V36[0] | |
| 14th Parameter | 1 | ↑ | 1 | - | - | - | - | - | PVR3 V43[3] | PVR3 V43[2] | PVR3 V43[1] | PVR3 V43[0] | |

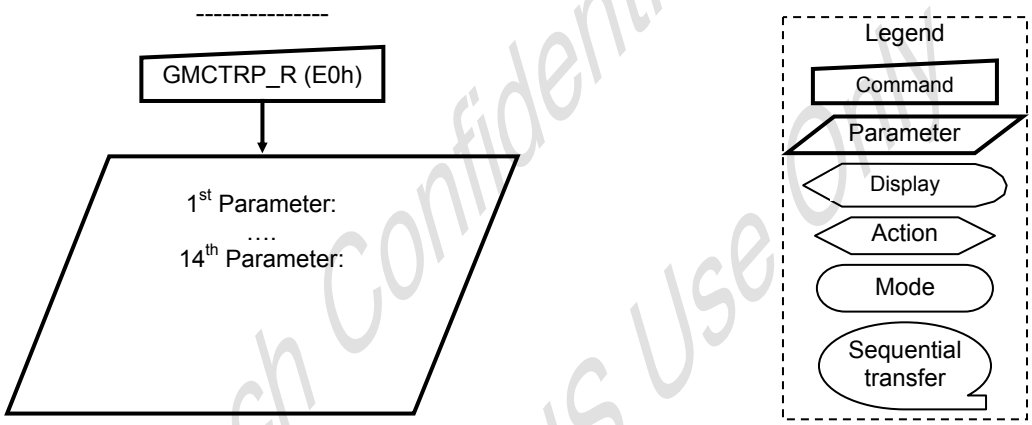
*NOTE: "-" Don't care*

| | |
|---|---|
| Description | -The default vaule for gamma register is for MVA LC type, GAMMA curve 2.2.<br>-The gamma volatge<br>  |
| Restriction | |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

Flow Chart



### 6.3.22. GMCTRN (E1h): Gamma Correction Characteristics Setting

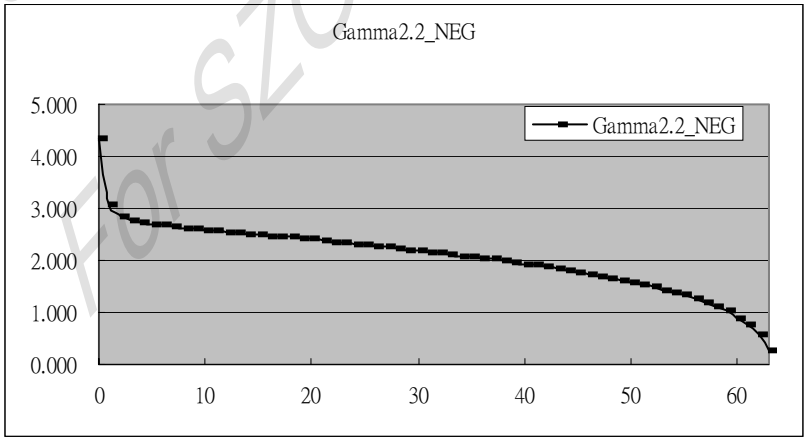
| E1H | GMCTRN1 (Gamma '-'polarity Correction Characteristics Setting) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Inst / Para | D/CX | WRX | RDX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (Code) |
| GMCTRN1 | 0 | ↑ | 1 | - | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | (E1h) |
| 1st Parameter | 1 | ↑ | 1 | - | - | - | - NVR1 V0[5] | NVR1 V0[4] | NVR1 V0[3] | NVR1 V0[2] | NVR1 V0[1] | NVR1 V0[0] | |
| 2nd Parameter | 1 | ↑ | 1 | - | - | - | NVR1 V1[5] | NVR1 V1[4] | NVR1 V1[3] | NVR1 V1[2] | NVR1 V1[1] | NVR1 V1[0] | |
| 3rd Parameter | 1 | ↑ | 1 | - | - | - | NVR1 V2[5] | NVR1 V2[4] | NVR1 V2[3] | NVR1 V2[2] | NVR1 V2[1] | NVR1 V2[0] | |
| 4th Parameter | 1 | ↑ | 1 | - | - | - | NVR1 V61[5] | NVR1 V61[4] | NVR1 V61[3] | NVR1 V61[2] | NVR1 V61[1] | NVR1 V61[0] | |
| 5th Parameter | 1 | ↑ | 1 | - | - | - | NVR1 V62[5] | NVR1 V62[4] | NVR1 V62[3] | NVR1 V62[2] | NVR1 V62[1] | NVR1 V62[0] | |
| 6th Parameter | 1 | ↑ | 1 | - | - | - | NVR1 V63[5]- | NVR1 V63[4] | NVR1 V63[3] | NVR1 V63[2] | NVR1 V63[1] | NVR1 V63[0] | |
| 7th Parameter | 1 | ↑ | 1 | - | - | - | NVR2 V13[5] | NVR2 V13[4] | NVR2 V13[3] | NVR2 V13[2] | NVR2 V13[1] | NVR2 V13[0] | |
| 8th Parameter | 1 | ↑ | 1 | - | - | - | NVR2 V50[5] | NVR2 V50[4] | NVR2 V50[3] | NVR2 V50[2] | NVR2 V50[1] | NVR2 V50[0] | |
| 9th Parameter | 1 | ↑ | 1 | - | - | - | - | - | NVR3 V4[3] | NVR3 V4[2] | NVR3 V4[1] | NVR3 V4[0] | |
| 10th Parameter | 1 | ↑ | 1 | - | - | - | - | - | NVR3 V8[3] | NVR3 V8[2] | NVR3 V8[1] | NVR3 V8[0] | |
| 11th Parameter | 1 | ↑ | 1 | - | - | - | - | - | NVR3 V20[3] | NVR3 V20[2] | NVR3 V20[1] | NVR3 V20[0] | |
| 12th Parameter | 1 | ↑ | 1 | - | - | - | - | - | NVR3 V27[3] | NVR3 V27[2] | NVR3 V27[1] | NVR3 V27[0] | |
| 13th Parameter | 1 | ↑ | 1 | - | - | - | - | - | NVR3 V36[3] | NVR3 V36[2] | NVR3 V36[1] | NVR3 V36[0] | |
| 14th Parameter | 1 | ↑ | 1 | - | - | - | - | - | NVR3 V43[3] | NVR3 V43[2] | NVR3 V43[1] | NVR3 V43[0] | |

*NOTE: "-" Don't care*

**Description**

-The default vaule for gamma register is for MVA LC type, GAMMA curve 2.2.

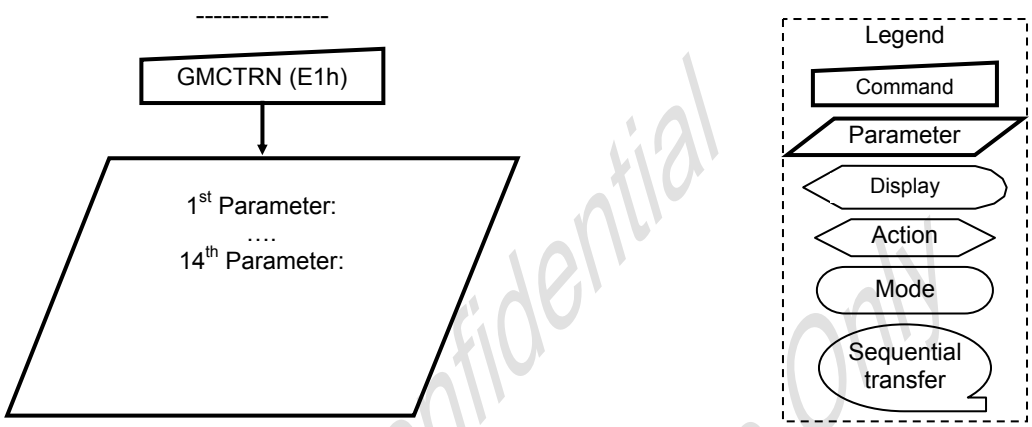
-The gamma volatge




**Restriction**

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

| | |
|---|---|
| Flow Chart |  |

## 7. FUNCTION DESCRIPTIONS

| MODE | | Interface Data | Interface Control Signal |
|---|---|---|---|
| 8080-MODE | 8-bits Parallel | D0~D7 | CSX<br>D/CX<br>WRX (R/WX)<br>RDX (E) |
| | 9-bits Parallel | D0~D8 | |
| | 16-bits Parallel | D0~D15 | |
| | 18-bits Parallel | D0~D17 | |
| 6800-MODE | 8-bits Parallel | D0~D7 | |
| | 9-bits Parallel | D0~D8 | |
| | 16-bits Parallel | D0~D15 | |
| | 18-bits Parallel | D0~D17 | |
| 3-Pin SPI | | D0 (SDA) | D/CX (SCL)<br>CSX |
| 4-Pin SPI | | D0 (SDA) | D/CX (SCL)<br>CSX<br>WRX (D/CX) |

Note 1 : In SPI I/F, D0 (Data bus bit 0) is used as Serial input/ output signal.(SDA)

Note 2 : In SPI I/F, D/CX is used as serial clock.(SCL)

Note 3 : In 4-Pin SPI I/F, WRX is used as data/command flag.( D/CX)

### 7.1. MPU Interface

#### 7.1.1. Interface Type Selection

The MPU interfaces of OTM3206A support 8-bit, 9-bit, 16-bit, and 18-bit's 80- or 68-system Interface and Serial Peripheral Interface (SPI), which can be set by the IM3/2/1/0 pins. The MPU interface can set instructions and access RAM. Table 7.2.1 depicts the interface corresponding to IM3/2/1/0 settings.

Table 7.2.1

| IM3 | IM2 | IM1 | IM0 | Interface | Read back selection |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 8080 MCU 8-bits Parallel | RDX strobe (8-bits read data and 8-bits read parameter) |
| 0 | 0 | 0 | 1 | 8080 MCU 9-bits Parallel | RDX strobe (9-bits read data and 8-bits read parameter) |
| 0 | 0 | 1 | 0 | 8080 MCU 16-bits Parallel | RDX strobe (16-bits read data and 8-bits read parameter) |
| 0 | 0 | 1 | 1 | 8080 MCU 18-bits Parallel | RDX strobe (18-bits read data and 8-bits read parameter) |
| 0 | 1 | 0 | 0 | 6800 MCU 8-bits Parallel | E strobe (8-bits read data and 8-bits read parameter) |
| 0 | 1 | 0 | 1 | 6800 MCU 9-bits Parallel | E strobe (9-bits read data and 8-bits read parameter) |
| 0 | 1 | 1 | 0 | 6800 MCU 16-bits Parallel | E strobe (16-bits read data and 8-bits read parameter) |
| 0 | 1 | 1 | 1 | 6800 MCU 18-bits Parallel | E strobe (18-bits read data and 8-bits read parameter) |
| 1 | 0 | 0 | 0 | 3-Pin Serial interface | Via the read instruction (8-bits, 24-bits and 32-bits read parameter |
| 1 | 0 | 0 | 1 | 4-Pin Serial interface | Via the read instruction (8-bits, 24-bits and 32-bits read parameter |

#### 7.1.2. 8080-Series Parallel interface(IM3='0' & IM2='0')

The MCU uses a 11-wires 8-data parallel interface or 19-wires 16-data parallel interface or 12-wires 9-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write, RDX is the parallel data read and D[17:0] is parallel data.

The Graphics Controller Chip reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/CX='0', D[17:0] bits are commands.

The 8080-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when IM2 pin is low state (VSS). Interface bus width can be selected with IM2, IM1 and IM0.

The interface function of 8080-series parallel interface are given in Table 7 2.2

Table 7.2.2 The function of 8080-series parallel interface

| IM3 | IM2 | IM1 | IM0 | Interface | D/CX | RDX | WRX | Function |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 8-bits Parallel | 0 | 1 | ↑ | Write 8-bits command (D7 to D0) |
| | | | | | 1 | 1 | ↑ | Write 8-bits display data or 8-bits parameter (D7 to D0) |
| | | | | | 1 | ↑ | 1 | Read 8-bits command (D7 to D0) |
| | | | | | 1 | ↑ | 1 | Read 8-bits parameter or status (D7 to D0) |
| 0 | 0 | 1 | 0 | 16-bits Parallel | 0 | 1 | ↑ | Write 8-bits command (D7 to D0) |
| | | | | | 1 | 1 | ↑ | Write 16-bits display data (D15 to D0) or 8-bits parameter (D7 to D0) |
| | | | | | 1 | ↑ | 1 | Read 8-bits command (D7 to D0) |
| | | | | | 1 | ↑ | 1 | Read 8-bits parameter or status (D7 to D0) |
| 0 | 0 | 0 | 1 | 9-bits Parallel | 0 | 1 | ↑ | Write 8-bits command (D7 to D0) |
| | | | | | 1 | 1 | ↑ | Write 9-bits display data (D8 to D0) or 8-bits parameter (D7 to D0) |
| | | | | | 1 | ↑ | 1 | Read 8-bits command (D7 to D0) |
| | | | | | 1 | ↑ | 1 | Read 8-bits parameter or status (D7 to D0) |
| 0 | 0 | 1 | 1 | 18-bits Parallel | 0 | 1 | ↑ | Write 8-bits command (D7 to D0) |
| | | | | | 1 | 1 | ↑ | Write 18-bits display data (D17 to D0) or 8-bits parameter (D7 to D0) |
| | | | | | 1 | ↑ | 1 | Read 8-bits command (D7 to D0) |
| | | | | | 1 | ↑ | 1 | Read 8-bits parameter or status (D7 to D0) |

### 7.1.2.1. Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (D/CX, RDX, WRX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data ('1').

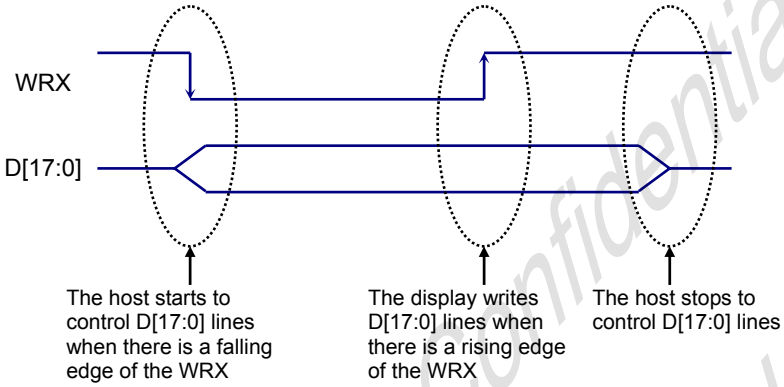



Fig. 7.2.2.1.1 8080-Series WRX Protocol

*Note: WRX is an unsynchronized signal (It can be stopped)*

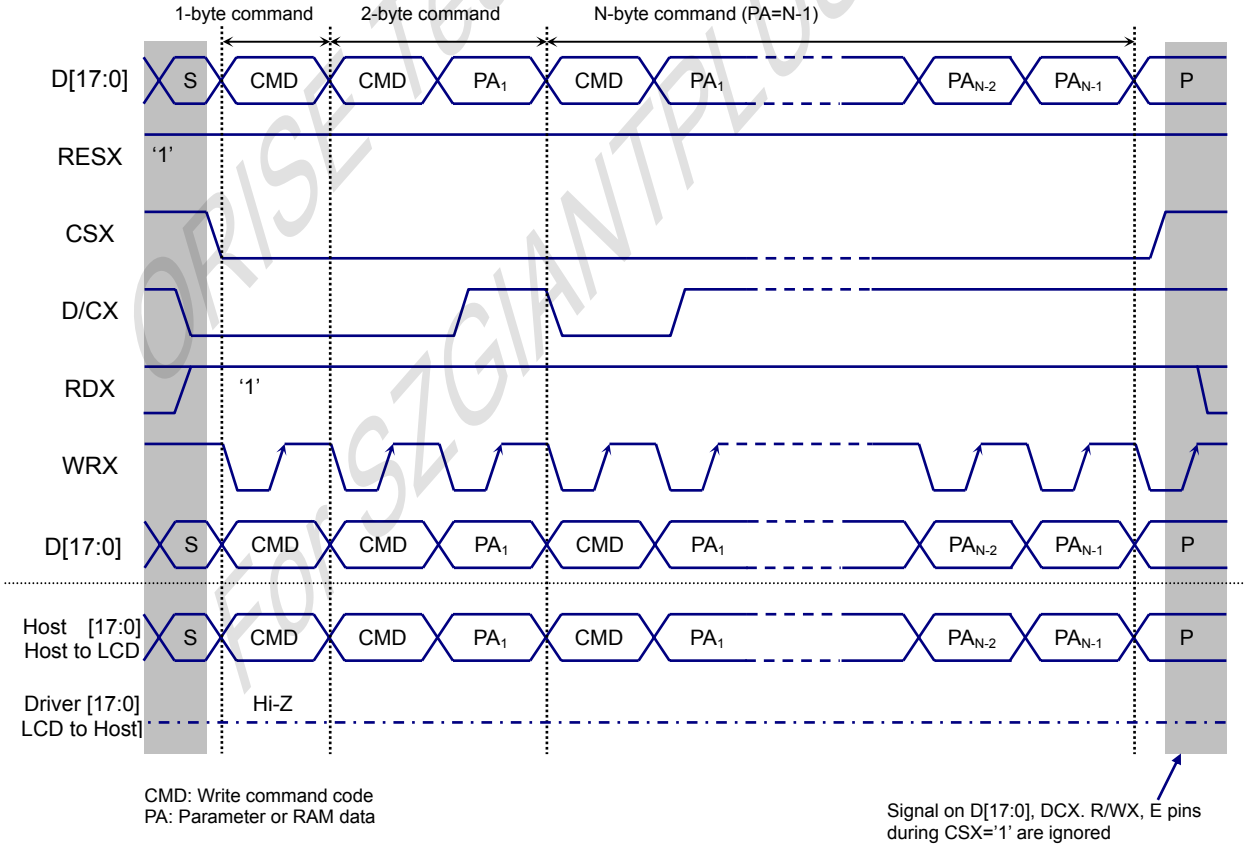



Fig. 7.2.2.1.2 8080-Series parallel bus protocol, Write to register or display RAM

### 7.1.2.2. Read Cycle Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The display sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

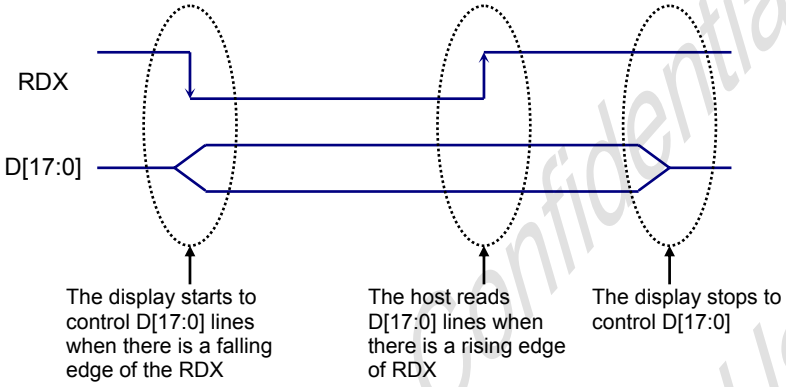



Fig. 7.2.2.2.1 8080-Series RDX Protocol

*Note: RDX is an unsynchronized signal (It can be stopped)*

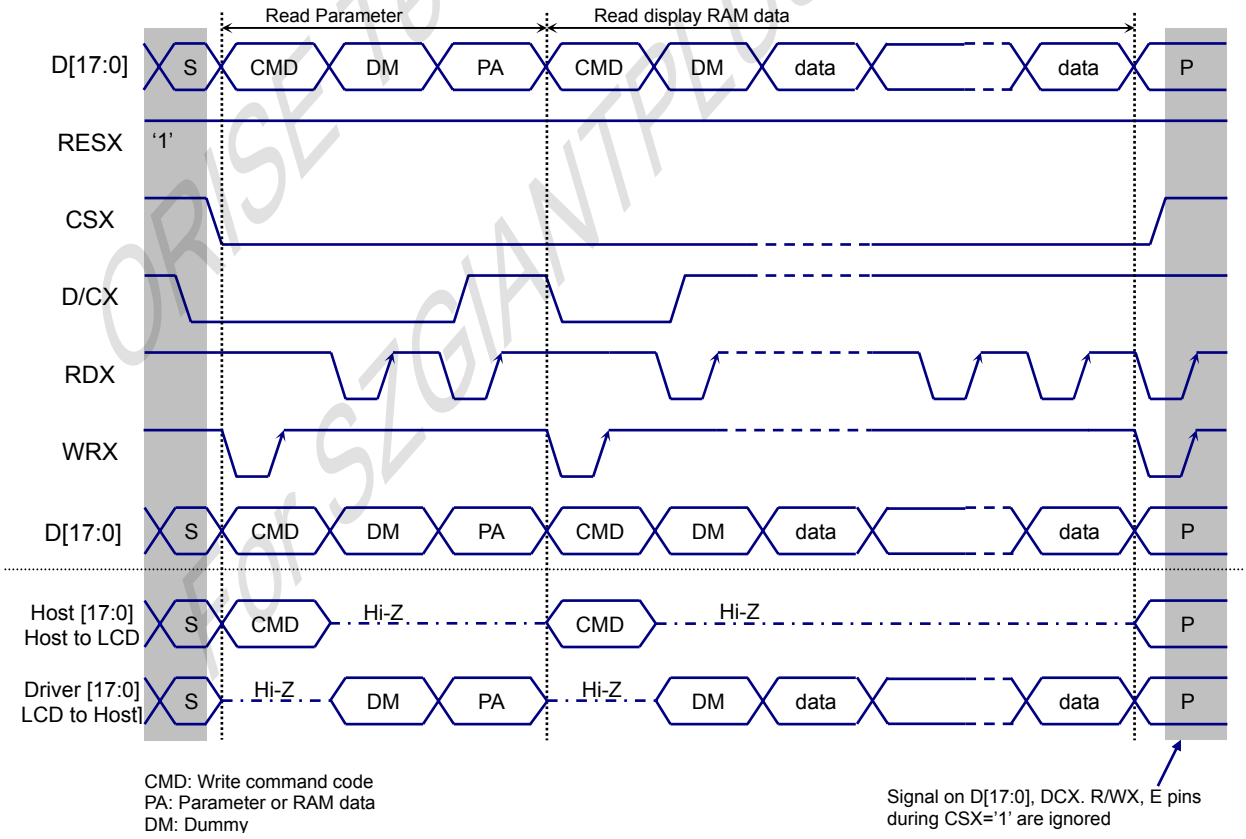



Fig. 7.2.2.2.2 8080-Series parallel bus protocol, Read data from register or display RAM

### 7.1.3. 6800-Series Parallel Interface (IM2='1' & IM3='0')

The MCU uses a 11-wires 8-data parallel interface or 19-wires 16-data parallel interface or 12-wires 9-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. The R/WX is the Read/Write flag and D[17:0] is parallel data.

The Graphics Controller Chip reads the data at the falling edge of E signal when R/WX='1' and Writes the data at the falling of the E signal when R/WX='0'. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C='0', D[17:0] bits are commands.

The 6800-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when IM2 pin is high state (VDDIO). Interface bus width can be selected with IM2, IM1 and IM0.

The interface functions of 6800-series parallel interface are given in Table 7.2.3.

Table 7.2.3 The function of 6800-series parallel interface

| IM3 | IM2 | IM1 | IM0 | Interface | D/CX | R/WX | E | Function |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 8-bits Parallel | 0 | 0 | ↓ | Write 8-bits command (D7 to D0) |
| | | | | | 1 | 0 | ↓ | Write 8-bits display data or 8-bits parameter (D7 to D0) |
| | | | | | 1 | 1 | ↓ | Read 8-bits command (D7 to D0) |
| | | | | | 1 | 1 | ↓ | Read 8-bits parameter or status (D7 to D0) |
| 0 | 1 | 1 | 0 | 16-bits Parallel | 0 | 0 | ↓ | Write 8-bits command (D7 to D0) |
| | | | | | 1 | 0 | ↓ | Write 16-bits display data (D15 to D0) or 8-bits parameter (D7 to D0) |
| | | | | | 1 | 1 | ↓ | Read 8-bits command (D7 to D0) |
| | | | | | 1 | 1 | ↓ | Read 8-bits parameter or status (D7 to D0) |
| 0 | 1 | 0 | 1 | 9-bits Parallel | 0 | 0 | ↓ | Write 8-bits command (D7 to D0) |
| | | | | | 1 | 0 | ↓ | Write 9-bits display data (D8 to D0) or 8-bits parameter (D7 to D0) |
| | | | | | 1 | 1 | ↓ | Read 8-bits command (D7 to D0) |
| | | | | | 1 | 1 | ↓ | Read 8-bits parameter or status (D7 to D0) |
| 0 | 1 | 1 | 1 | 18-bits Parallel | 0 | 0 | ↓ | Write 8-bits command (D7 to D0) |
| | | | | | 1 | 0 | ↓ | Write 18-bits display data (D17 to D0) or 8-bits parameter (D7 to D0) |
| | | | | | 1 | 1 | ↓ | Read 8-bits command (D7 to D0) |
| | | | | | 1 | 1 | ↓ | Read 8-bits parameter or status (D7 to D0) |

### 7.1.3.1. Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

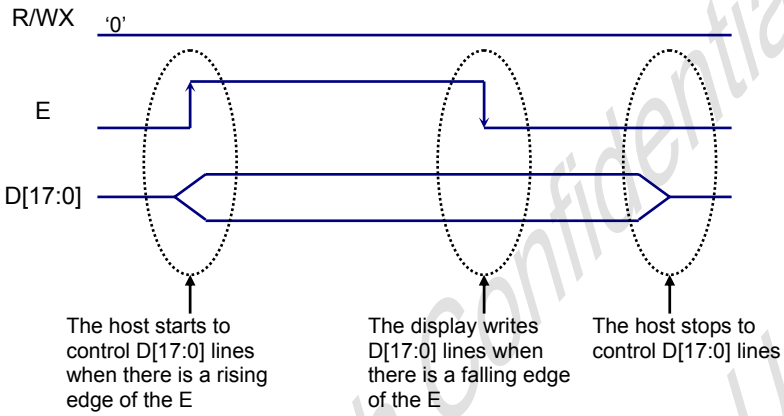



Fig. 7.2.3.1.1 6800-Series Write Protocol

*Note: E is an unsynchronized signal (It can be stopped)*

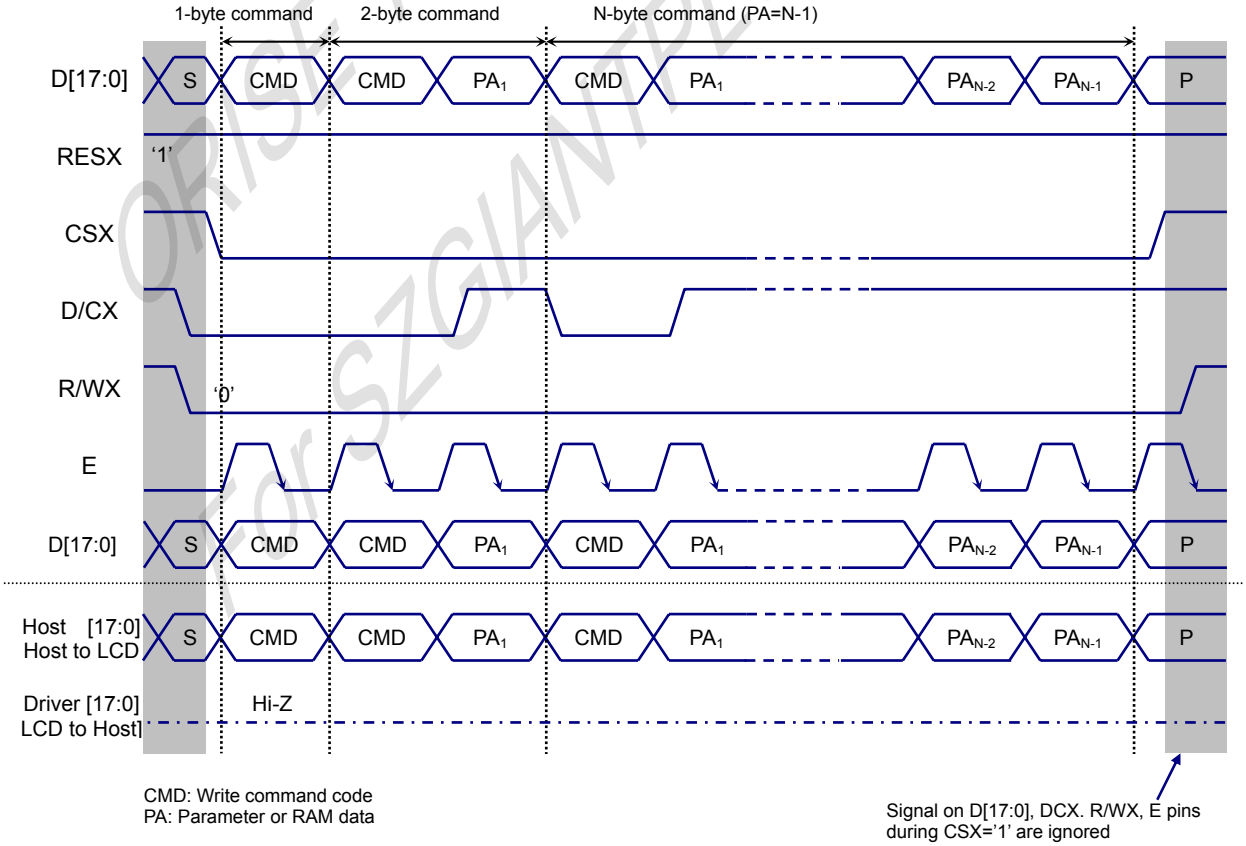



Fig. 7.2.3.1.2 6800-Series parallel bus protocol, Write to register or display RAM

### 7.1.3.2. Read cycle sequence

The read cycle means that the host reads information (command or/and data) to the display via the interface. Each read cycle (E low-high-low sequence) consists of 3 control (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

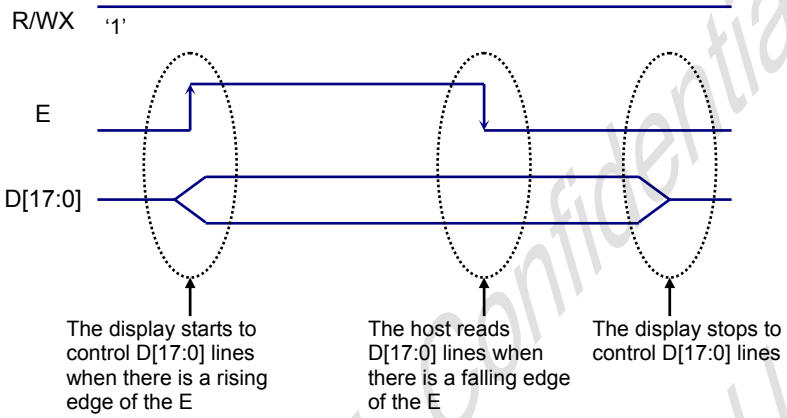



Fig. 7.2.3.2.1 6800-Series Read Protocol

*Note: E is an unsynchronized signal (It can be stopped)*

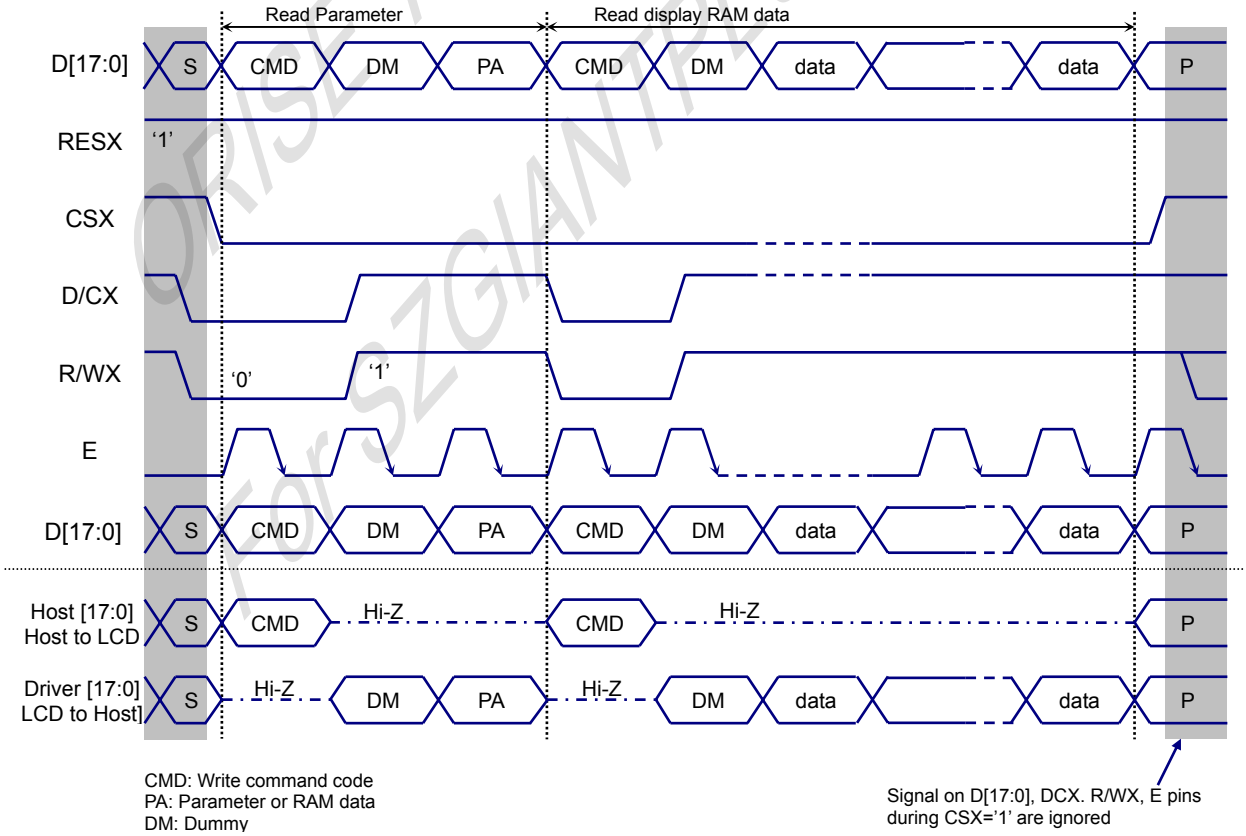



Fig. 7.2.3.2.2 6800-Series parallel bus protocol, Read data from register or display RAM

### 7.1.4. Serial Peripheral interface

#### 7.1.4.1. 3-pin 9-bits SPI

The selection of this interface is done by IM2 and IM3. See the Table 7.2.4.1.

The serial interface is a 3-pin 9-bits bi-directional interface for communication between the micro controller and the LCD driver chip. The 3-pin serial use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

Table 7.2.4.1 Serial Interface Type Selection

| IM3 | IM2 | IM1 | IM0 | Interface | Read back selection |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 3-Pin Serial interface | Via the read instruction (8-bits, 24-bits and 32-bits read parameter |

#### 7.1.4.1.1. Command Write Mode

The write mode of the interface means the micro controller writes commands and data to the 3-Pin serial data packet contains a control bit D/CX and a transmission byte. If D/CX is low, the transmission byte is interpreted as command byte. If D/CX is high, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to the DRIVER. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

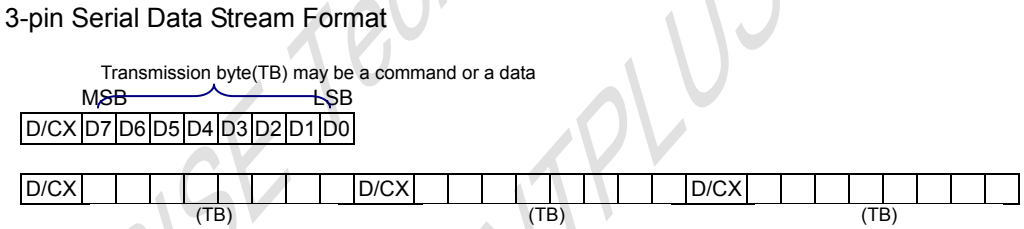



Fig. 7.2.4.1.1 Serial interface data Stream format

When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low. SDA is sampled at the rising edge of CSX. D/CX indicates, whether the byte is command code (D/CX='0') or parameter/RAM data (D/CX='1'). It is sampled when first rising edge of CSX. If CSX stay low after the last bit of command/data byte, the serial interface expects the D/CX bit of the next byte at the next rising edge of SCL.

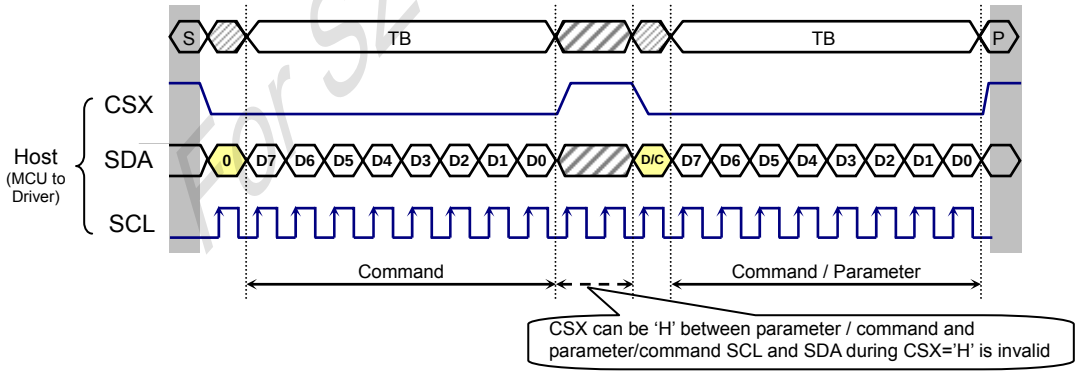
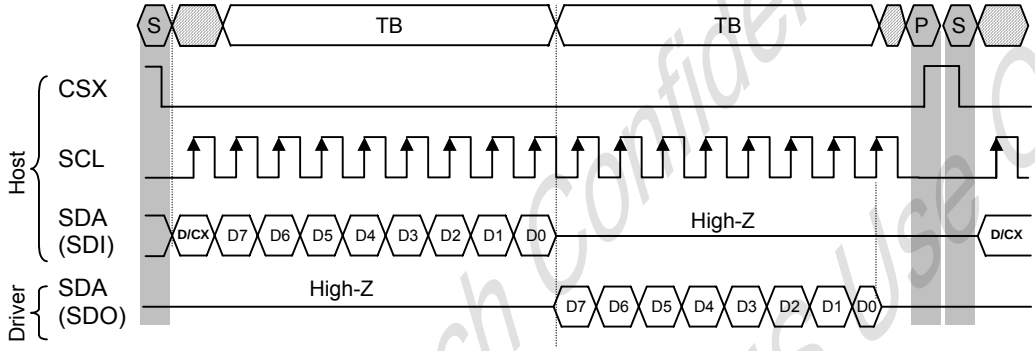



Fig. 7.2.4.1.2 Serial interface Write protocol (Write to register with control bit in transmission)

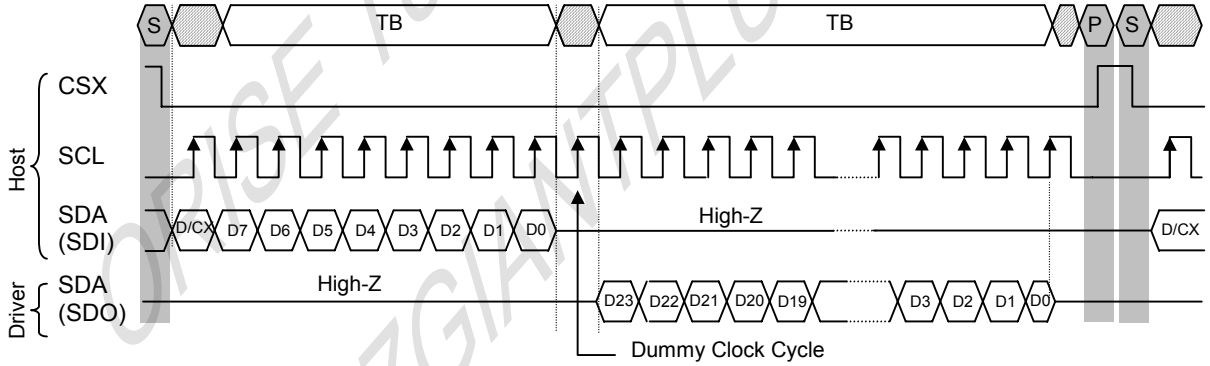
#### 7.1.4.1.2. Read Functions

The read mode of the interface means that the micro controller reads register value from the Driver. To do the micro controller first has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. After the read status command has been sent, the SDA lin must be set to tri-state no later than at the falling edge of SCL of the last bit.

3-Pin Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)




3-Pin Serial Protocol (for RDDID command: 24-bit read)




3-Pin Serial Protocol (for RDDST command: 32-bit read)

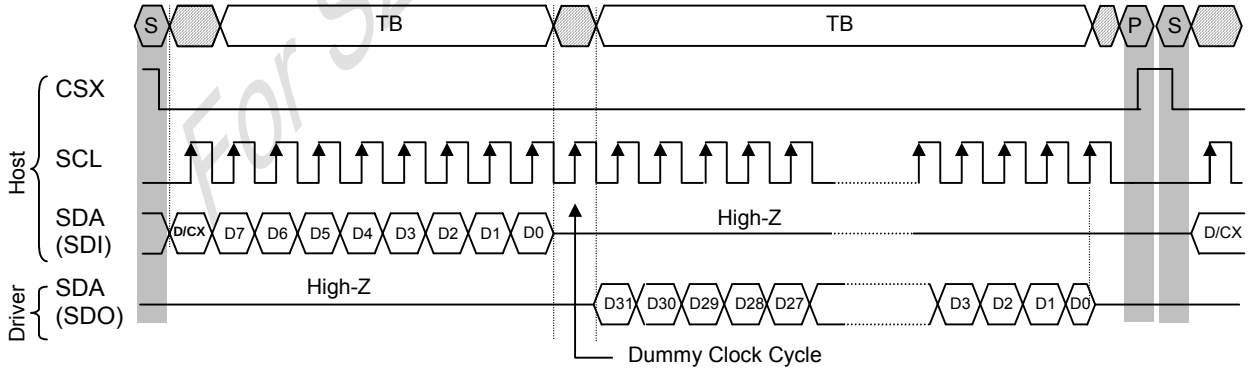



Fig. 7.2.4.1.2 3-pin Serial interface Read protocol

### 7.1.4.2. 4-pin 8-bits SPI

The selection of this interface is done by IM2 and IM3. See the Table 7.2.4.2.

The serial interface is a 4-pin 8-bits bi-directional interface for communication between the micro controller and the LCD driver chip. The 4-pin serial use: CSX (chip enable), SCL (serial clock), DCX(command or data) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

Table 7.2.4.2 Serial Interface Type Selection

| IM3 | IM2 | IM1 | IM0 | Interface | Read back selection |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 4-Pin Serial interface | Via the read instruction (8-bits, 24-bits and 32-bits read parameter |

#### 7.1.4.2.1. Command Write Mode

The write mode of the interface means the micro controller writes commands and data to the 4-Pin serial data packet. If D/CX is low, the transmission byte is interpreted as command byte. If D/CX is high, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to the DRIVER. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

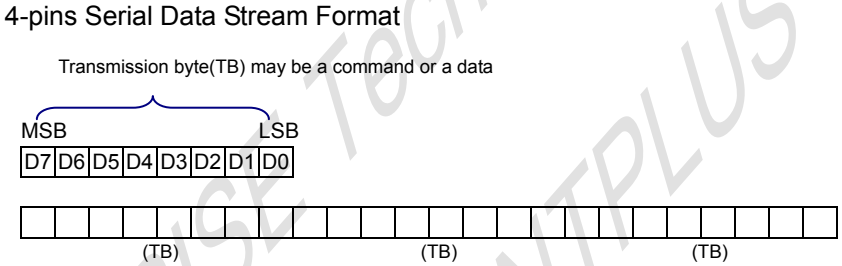



Fig. 7.2.4.2.1 Serial interface data Stream format

When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low. SDA is sampled at the rising edge of CSX. D/CX indicates, whether the byte is command code (D/CX='0') or parameter/RAM data (D/CX='1'). It is sampled when first rising edge of CSX. If CSX stay low after the last bit of command/data byte, the serial interface expects the D/CX bit of the next byte at the next rising edge of SCL.

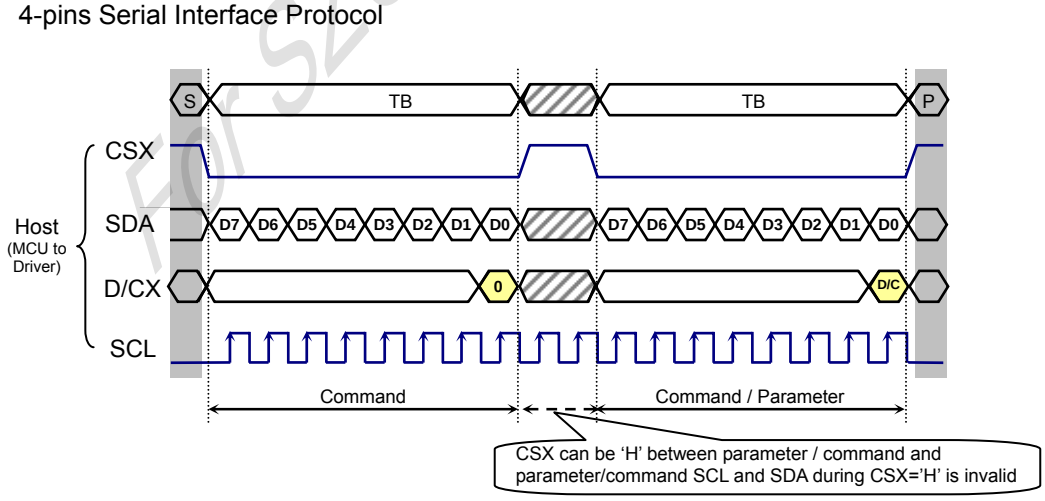
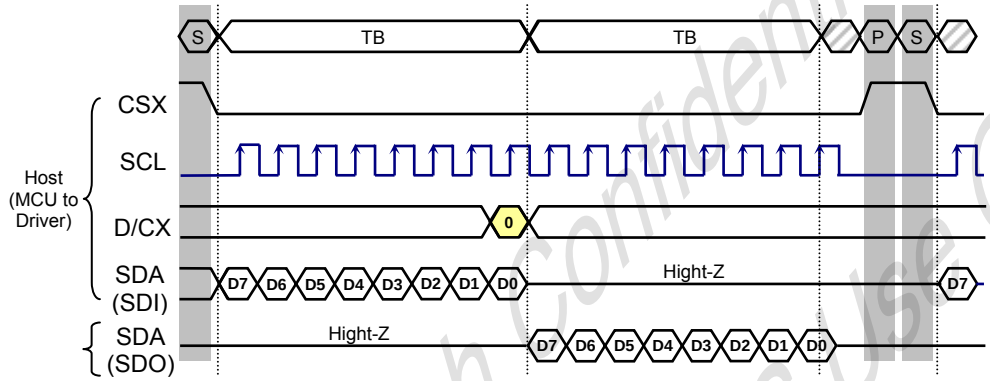



Fig. 7.2.4.2.2 4-pins Serial interface Write protocol (Write to register with control bit in

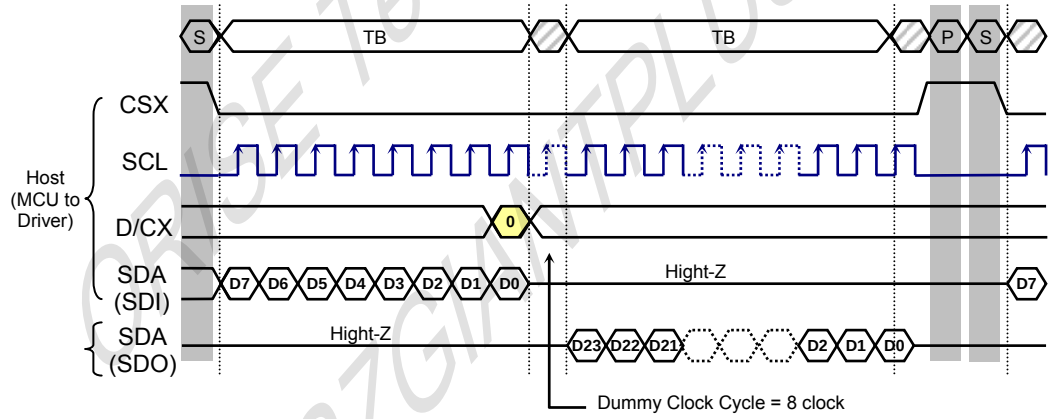
#### 7.1.4.2.2. Read Functions

The read mode of the interface means that the micro controller reads register value from the Driver. To do the micro controller first has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. After the read status command has been sent, the SDA lin must be set to tri-state no later than at the falling edge of SCL of the last bit.

4-pins Serial Protocol (for RDID1/ RDID2/ RDID3/ 0AH/ 0BH/ 0CH/ 0DH/ 0EH/ 0FH command: 8-bits read)




4-pins Serial Protocol (for RDDID command: 24-bits read)




4-pins Serial Protocol (for RDDST command: 32-bits read)

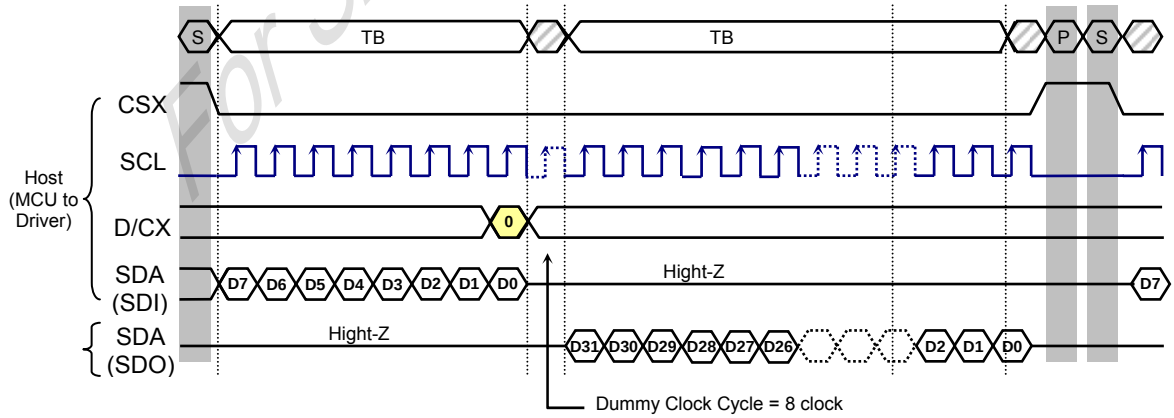



Fig. 7.2.4.2.2 4-pins Serial interface Read protocol

### 7.1.5. Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then DRIVER will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been High state. See the following example

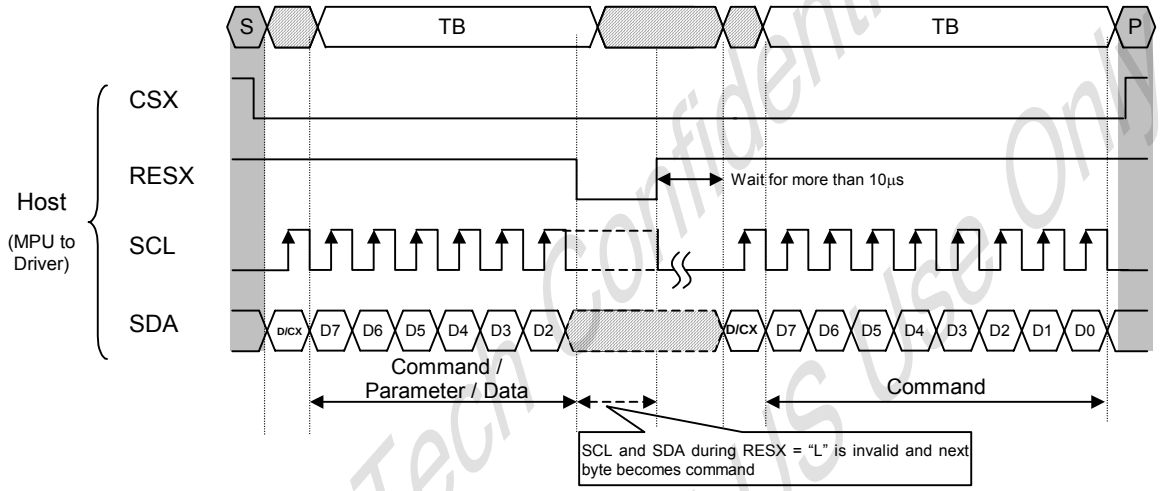



Fig. 7.2.5.1 Serial bus protocol, write mode – interrupted by RESX

If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then DRIVER will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example

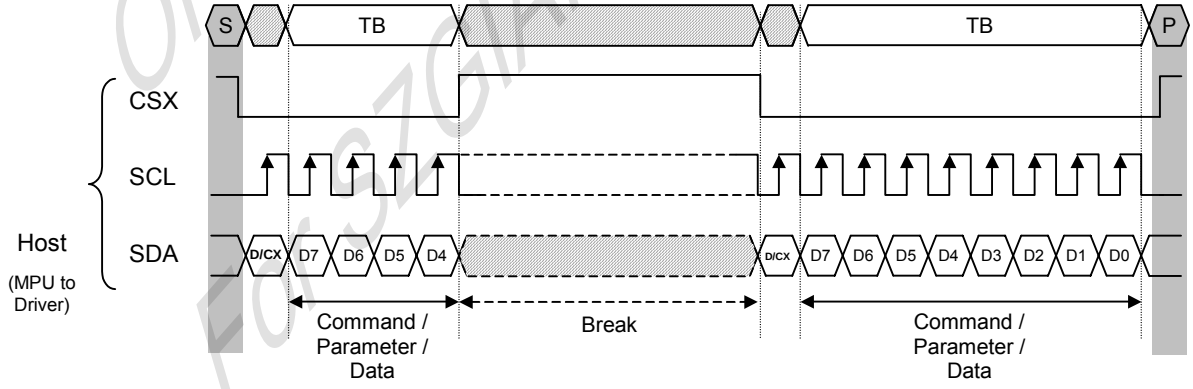



Fig. 7.2. 5.2 Serial bus protocol, write mode – interrupted by CSX

If 1, 2 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

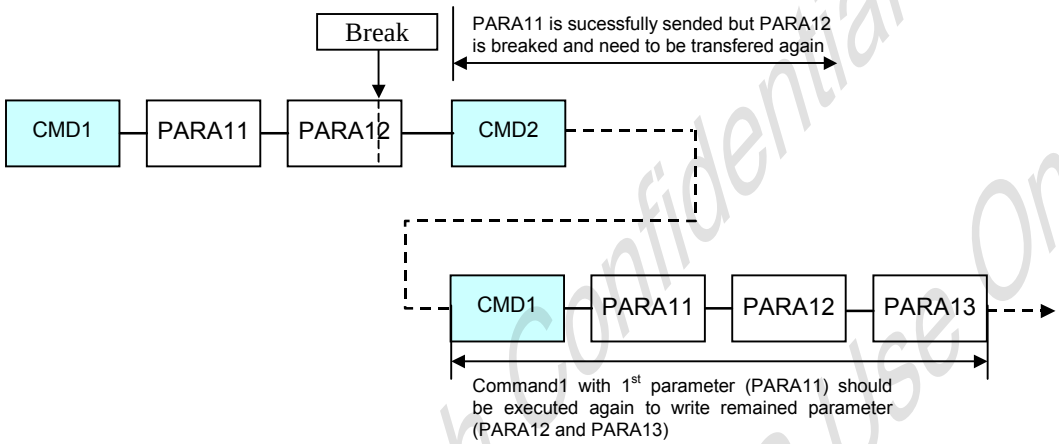



Fig.7.2.5.3 Write interrupts recovery (serial interface)

If a 2 or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

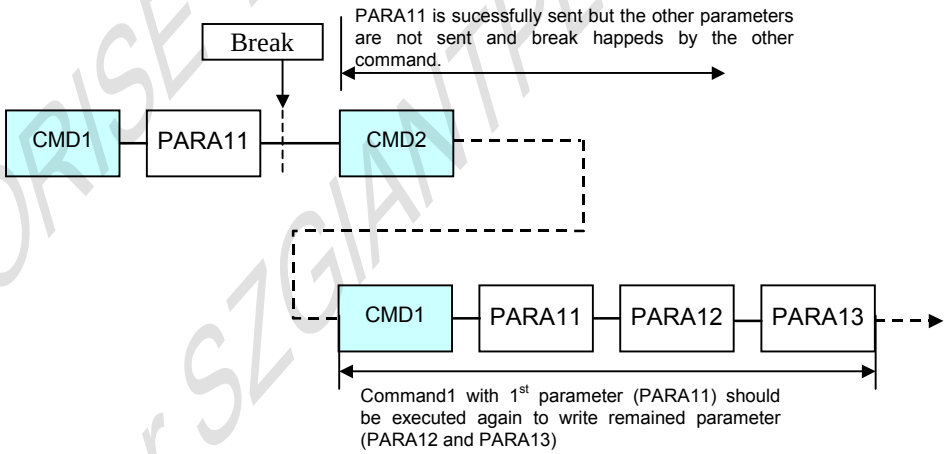



Fig. 7.2.5.4 Write interrupts recovery (both serial and parallel interface)

### 7.1.6. Data Transfer Pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then DRIVER will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

This applies to the following 4 conditions:

1) Command-Pause-Command

2) Command-Pause-Parameter

3) Parameter-Pause-Command

4) Parameter-Pause-Parameter

#### 7.1.6.1. Serial Interface Pause

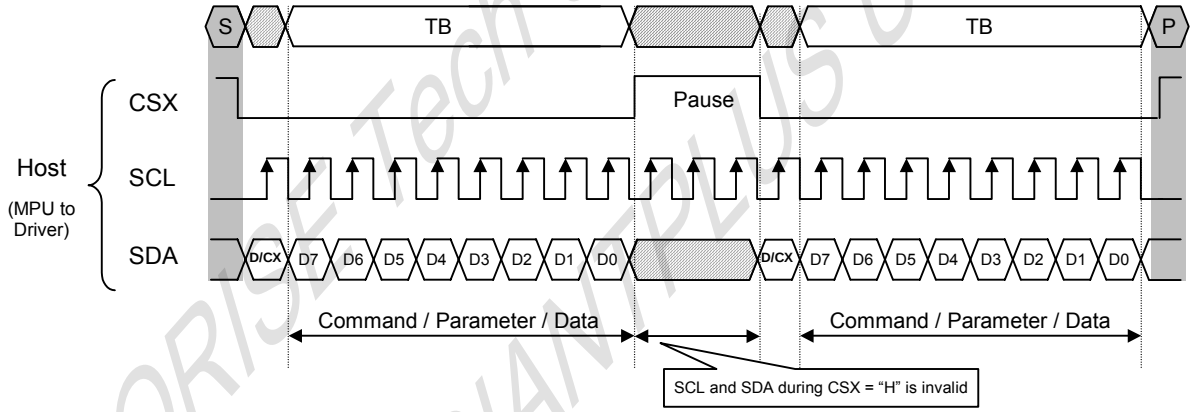



Fig. 7.2.6.1 Serial interface Pause Protocol (pause by CSX)

#### 7.1.6.2. Parallel Interface Pause

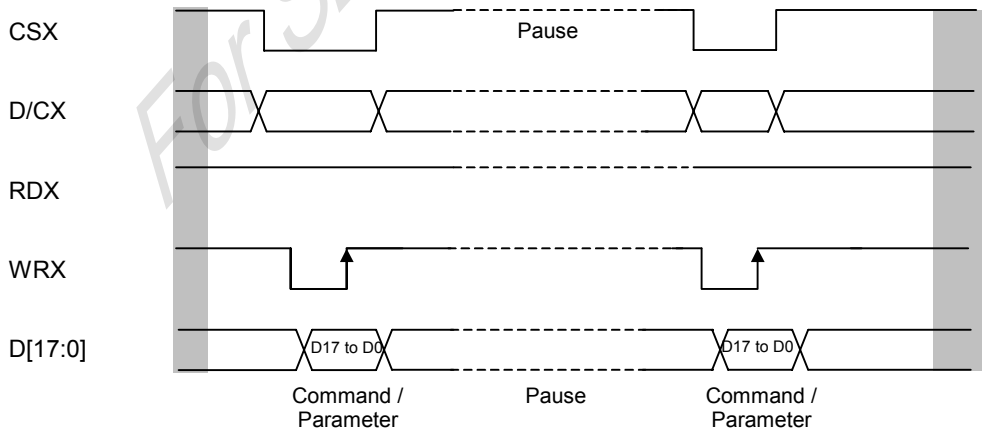


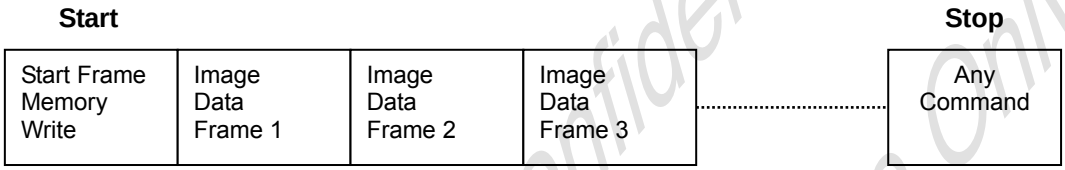

Fig. 7.2.6.2 Parallel bus Pause Protocol (paused by CSX)

### 7.1.7. Data Transfer Modes

The Module has three kinds colour modes for transferring data to the display RAM. These are 12-bit colour per pixel, 16-bit colour per pixel and 18-bit colour per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

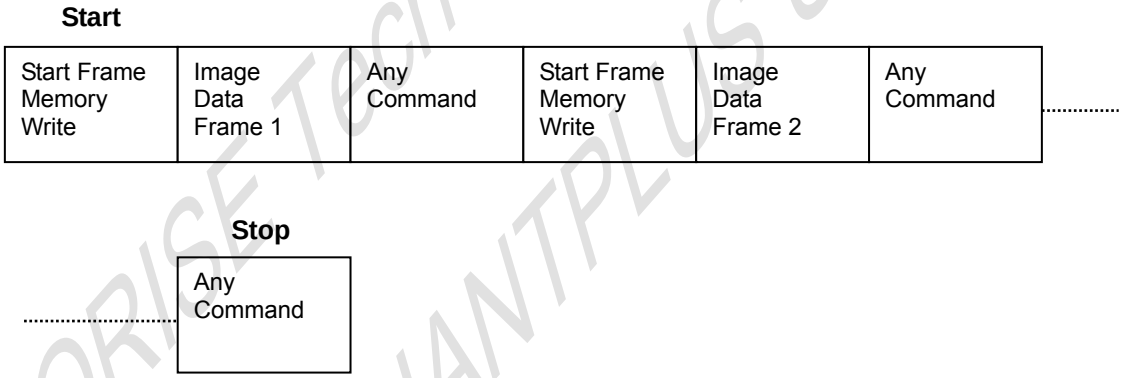
#### 7.1.7.1. Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.




#### 7.1.7.2. Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.




*Note:*

*1) These apply to all data transfer Colour modes on both serial and parallel interfaces.*

*2) The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.*

### 7.2. MCU Data Colour Coding

#### 7.2.1. MCU Data Colour Coding for RAM data ***Write***

- Parallel 8-Bits Bus Interface (IM1, IM0= "00")

Table 7.3.1.1 8-Bits Parallel Interface Set Table

| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | **2CH** |
| **3AH** | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Colour |
| 03h | x | x | x | x | x | x | x | x | x | x | R3 | R2 | R1 | R0 | G3 | G2 | G1 | G0 | 4K-Colour (2-pixels/ 3-byyes) |
| | x | x | x | x | x | x | x | x | x | x | B3 | B2 | B1 | B0 | R3 | R2 | R1 | R0 | |
| | x | x | x | x | x | x | x | x | x | x | G3 | G2 | G1 | G0 | B3 | B2 | B1 | B0 | |
| 05h | x | x | x | x | x | x | x | x | x | x | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | 65K-Colour (1-pixels/ 2-byyes) |
| | x | x | x | x | x | x | x | x | x | x | G2 | G1 | G0 | B4 | B3 | B2 | B1 | B0 | |
| 06h | x | x | x | x | x | x | x | x | x | x | R5 | R4 | R3 | R2 | R1 | R0 | x | x | 262K-Colour (1-pixels/ 3byyes) |
| | x | x | x | x | x | x | x | x | x | x | G5 | G4 | G3 | G2 | G1 | G0 | x | x | |
| | x | x | x | x | x | x | x | x | x | x | B5 | B4 | B3 | B2 | B1 | B0 | x | x | |

- Parallel 16-Bits Bus Interface (IM1, IM0= "10")

Table 7.3.1.2 16-Bits Parallel Interface Set Table

| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | **2CH** |
| **3AH** | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Colour |
| 03h | x | x | x | x | x | x | R3 | R2 | R1 | R0 | G3 | G2 | G1 | G0 | B3 | B2 | B1 | B0 | 4K-Colour |
| 05h | x | x | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B4 | B3 | B2 | B1 | B0 | 65K-Colour |
| 06h | x | x | R5 | R4 | R3 | R2 | R1 | R0 | x | x | G5 | G4 | G3 | G2 | G1 | G0 | x | x | 262K-Colour (2-pixels/ 3byyes) |
| | x | x | B5 | B4 | B3 | B2 | B1 | B0 | x | x | R5 | R4 | R3 | R2 | R1 | R0 | x | x | |
| | x | x | G5 | G4 | G3 | G2 | G1 | G0 | x | x | B5 | B4 | B3 | B2 | B1 | B0 | x | x | |

- Parallel 9-Bits Bus Interface (IM1, IM0= "01")

Table 7.3.1.3 9-Bits Parallel Interface Set Table

| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Register |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | **2CH** |
| **3AH** | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Colour |
| 06h | x | x | x | x | x | x | x | x | x | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | 262K-Colour (1-pixels/ 2bytes) |
| | x | x | x | x | x | x | x | x | x | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 | |

- Parallel 18-Bits Bus Interface (IM1, IM0= "11")

Table 7.3.1.4 18-Bits Parallel Interface Set Table

| **Register Command** | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Register |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | **2CH** |
| **3AH** | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Colour |
| 03h | x | x | x | x | x | x | R3 | R2 | R1 | R0 | G3 | G2 | G1 | G0 | B3 | B2 | B1 | B0 | **4K-Colour** |
| 05h | x | x | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B4 | B3 | B2 | B1 | B0 | **65K-Colour** |
| 06h | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 | **262K-Colour** |

*Note: 'x' Don't care, but need to set VDDIO or VSS level.*

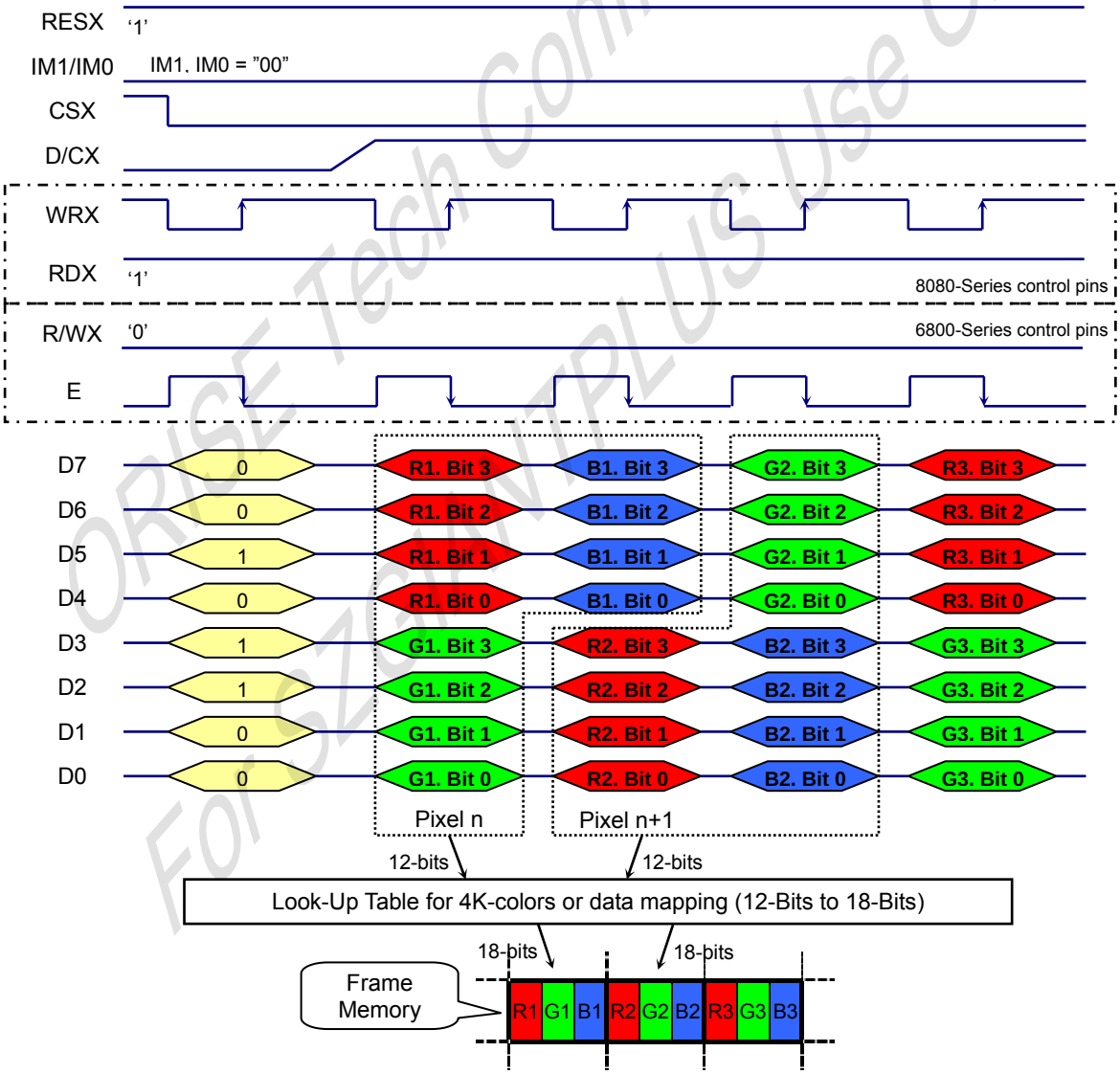
### 7.2.1.1. Parallel 8-Bits Bus Interface for RAM Data Write (IM1, IM0= “00”)

Different display data formats are available for three colours depth supported by listed below.

- 4K-Colours, RGB 4,4,4-bits input data. (3AH=”03h”)
- 65K-Colours, RGB 5,6,5-bits input data. (3AH=”05h”)
- 262K-Colours, RGB 6,6,6-bits input data. (3AH=”06h”)

(1). 8-bits data bus for 12-bits/pixel (RGB 4-4-4-bits input), 4K-colours, 3AH=”03h”

There are 2 pixels (6 sub-pixels) per 3-bytes.



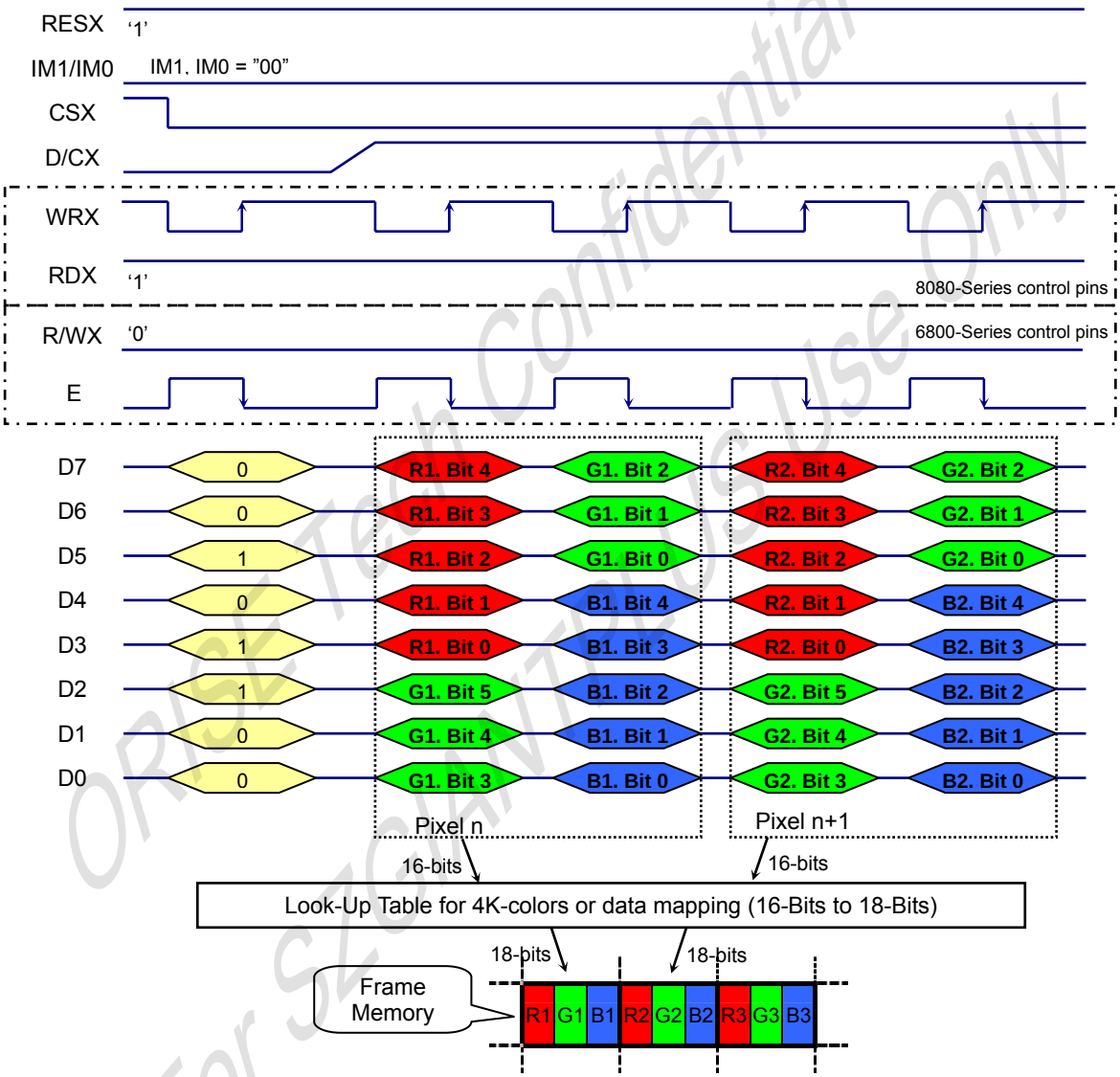

*Note1. The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.*

*Note 2.3-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.*

*Note 3. '-' = Don't care - Can be set to VDDIO or VSS level*

(2). 8-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colours, 3AH="05h"

There are 1 pixels (3 sub-pixels) per 2-bytes.



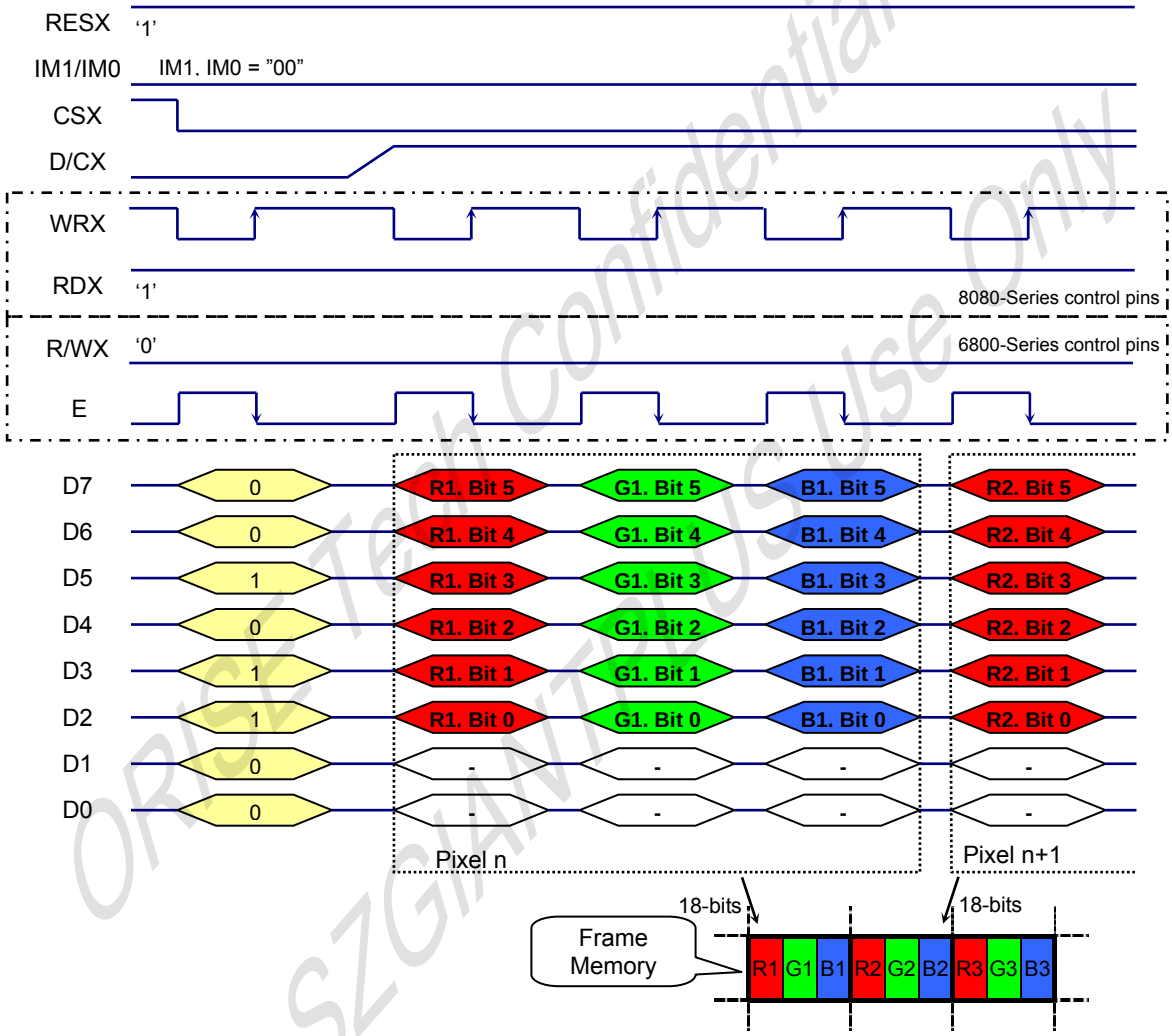

*Note1. The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.*

*Note 2.2-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.*

*Note 3. '-' = Don't care - Can be set to VDDIO or VSS level*

(3). 8-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colours, 3AH="06h"

There are 1 pixels (3 sub-pixels) per 3-bytes.




*Note1. The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.*
*Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.*
*Note 3. '-' = Don't care - Can be set to VDDIO or VSS level*

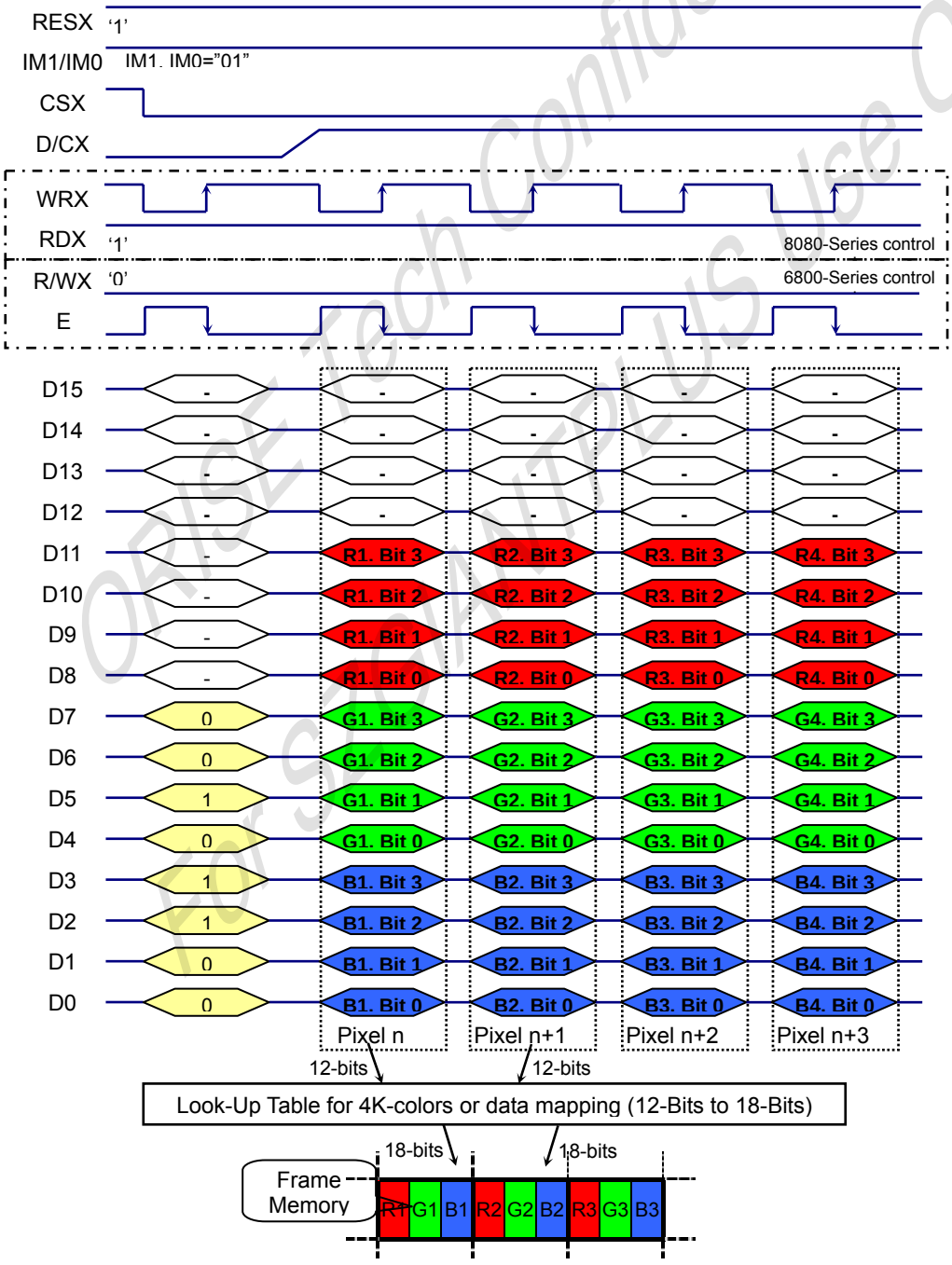
### 7.2.1.2. Parallel 16-Bits Bus Interface for RAM Data Write (IM1, IM0=”10”)

Different display data formats are available for three colors depth supported by listed below.

- 4K-Colours, RGB 4,4,4-bits input data. (3AH=”03h”)
- 65K-Colours, RGB 5,6,5-bits input data. (3AH=”05h”)
- 262K-Colours, RGB 6,6,6-bits input data. (3AH=”06h”)

(1). 16-bits data bus for 12-bits/pixel (RGB 4-4-4-bits input), 4K-colours, 3AH=”03h”

There are 1 pixel (3 sub-pixels) per 1 bytes



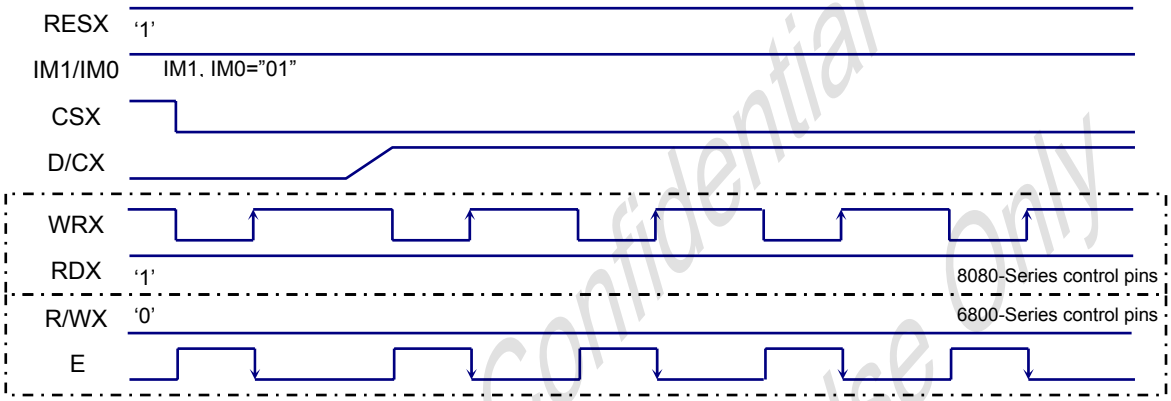

*Note1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.*

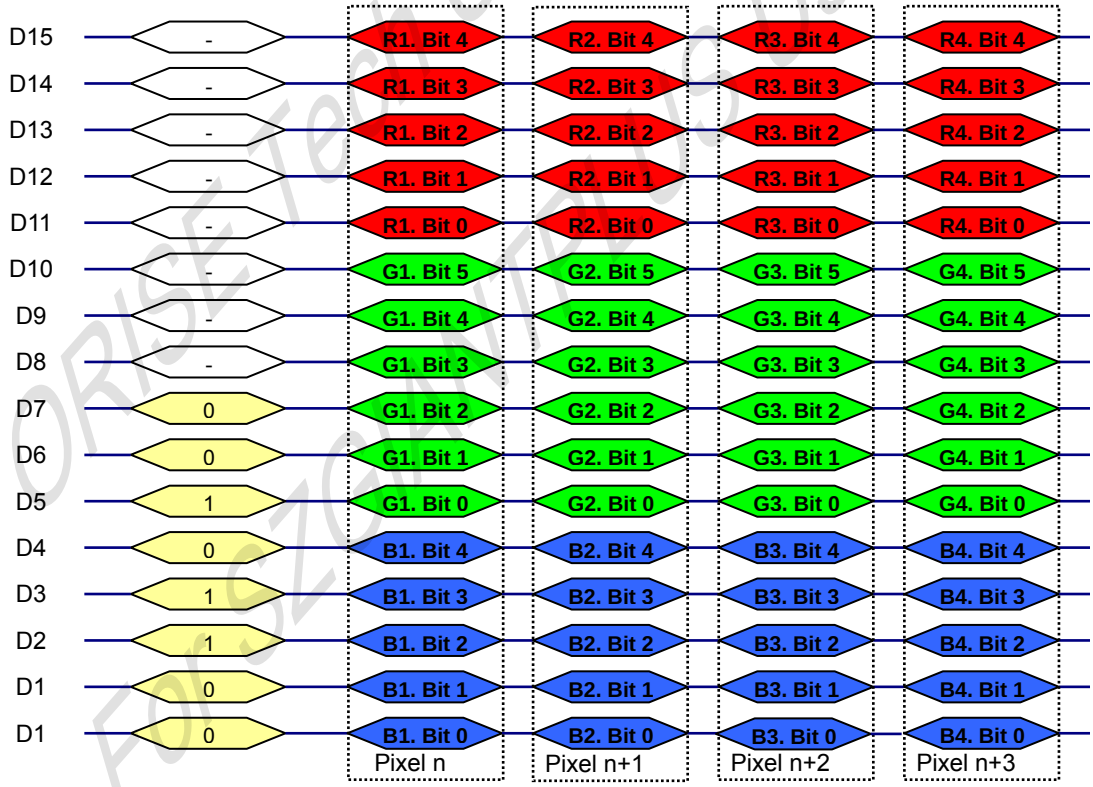
*Note 2.1-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.*

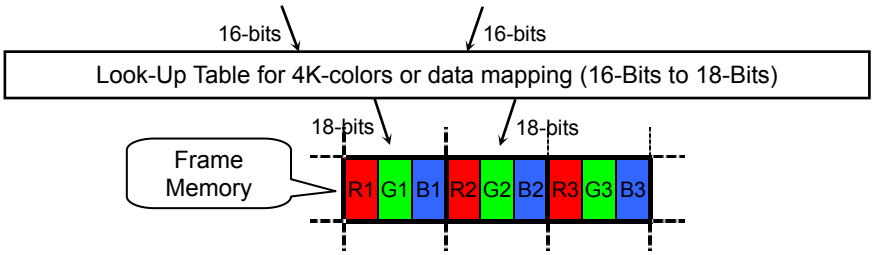
*Note 3. '-' = Don't care - Can be set to VDDIO or VSS level*

(2). 16-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colours, 3AH="05h"

There are 1 pixel (3 sub-pixels) per 1 bytes



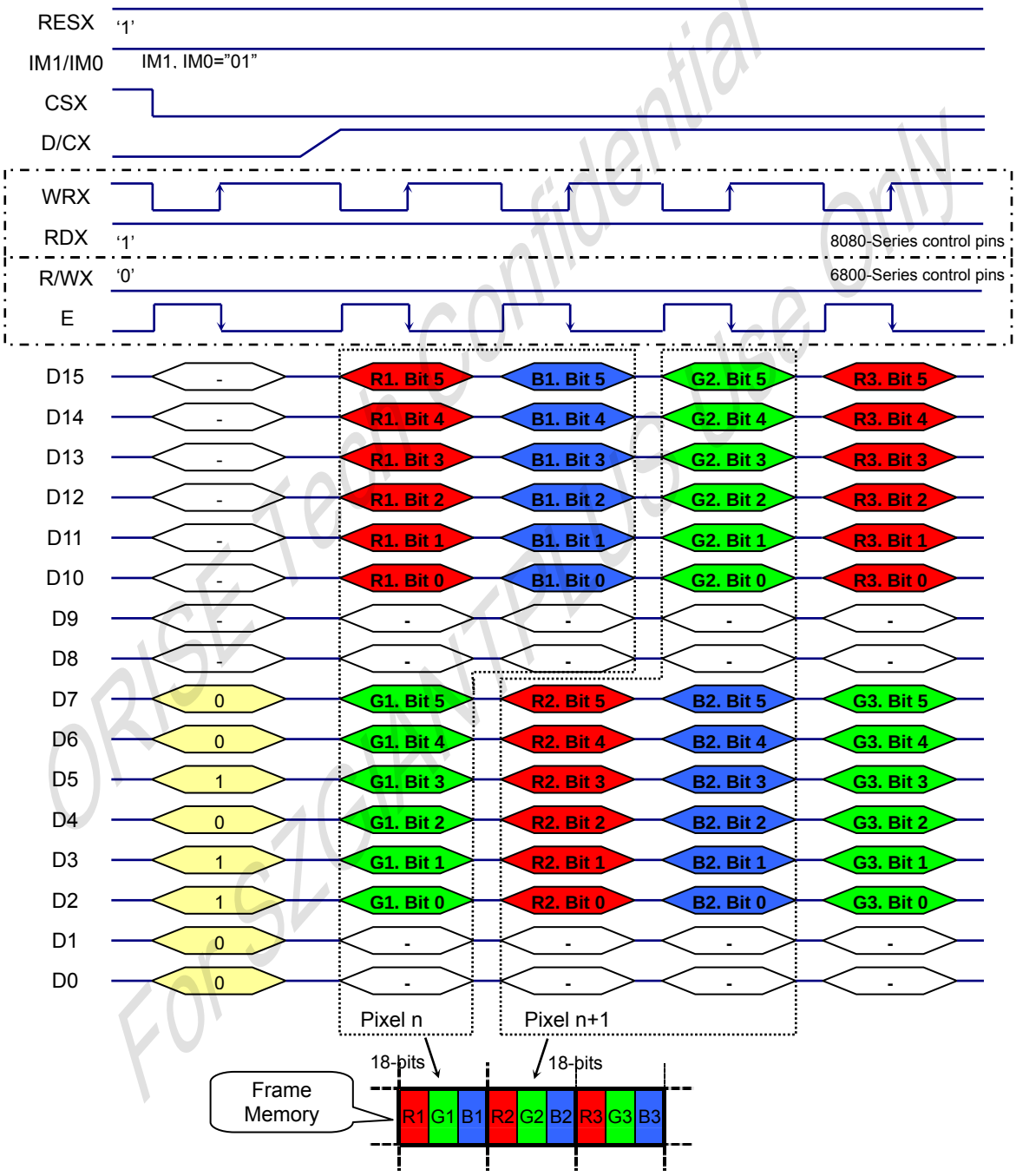

*Note1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.*

*Note 2.1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.*

*Note 3. '-' = Don't care - Can be set to VDDIO or VSS level*

(3). 16-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colours, 3AH="06h"

There are 2 pixel (6 sub-pixels) per 3 bytes






*Note1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.*

*Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.*

*Note 3. '-' = Don't care - Can be set to VDDIO or VSS level*

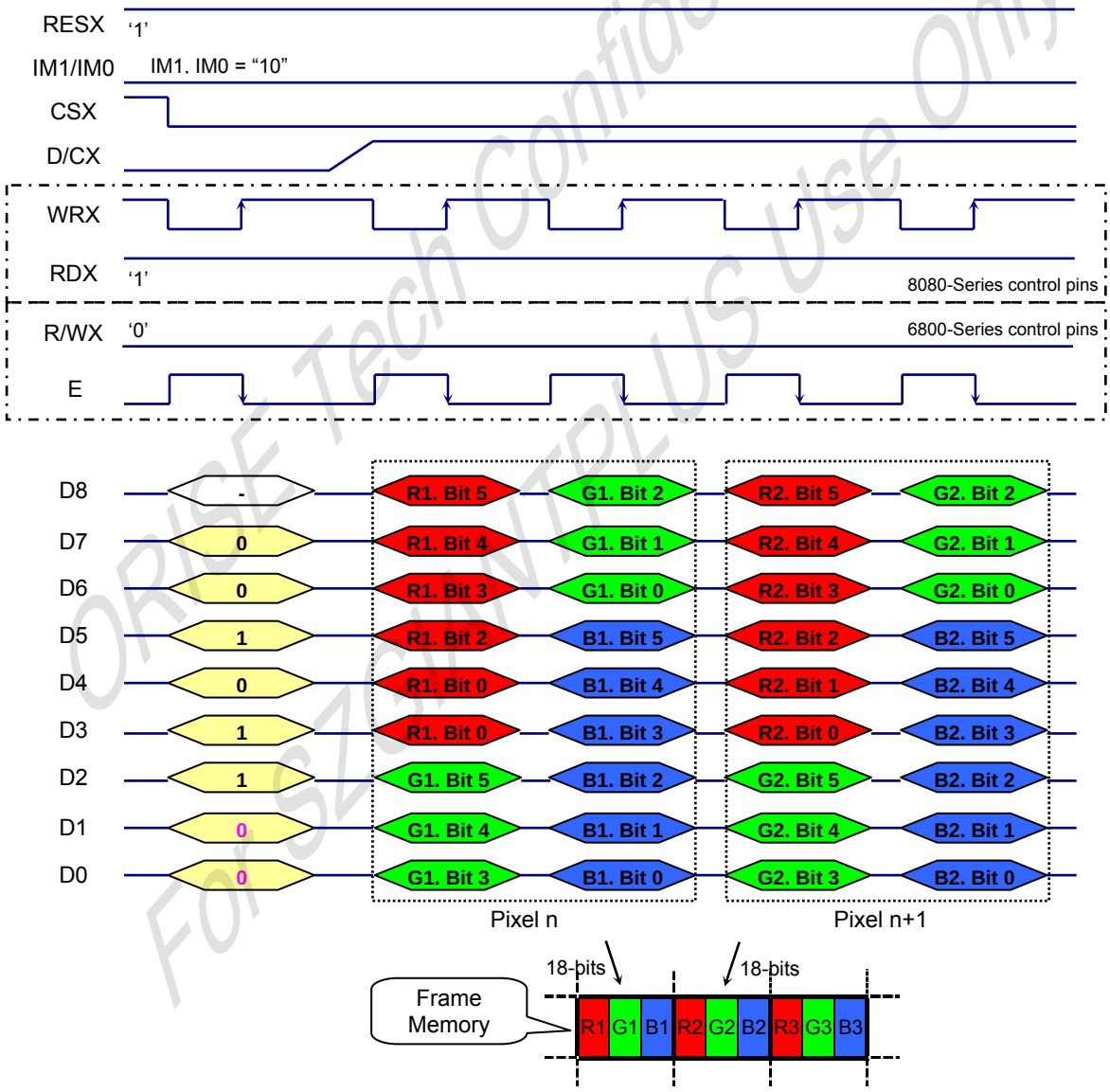
### 7.2.1.3. Parallel 9-Bits Bus Interface for RAM Data Write (IM1, IM0="01")

Different display data formats are available for three colors depth supported by listed below.

- 262K-Colours, RGB 6,6,6-bits input data. (3AH="06h")

(1). 9-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colours, 3AH="06h"

There is 1 pixel (3 sub-pixels) per 2 bytes




*Note1. The data order is ad follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.*

*Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.*

*Note 3. '-' = Don't care - Can be set to VDDIO or VSS level*

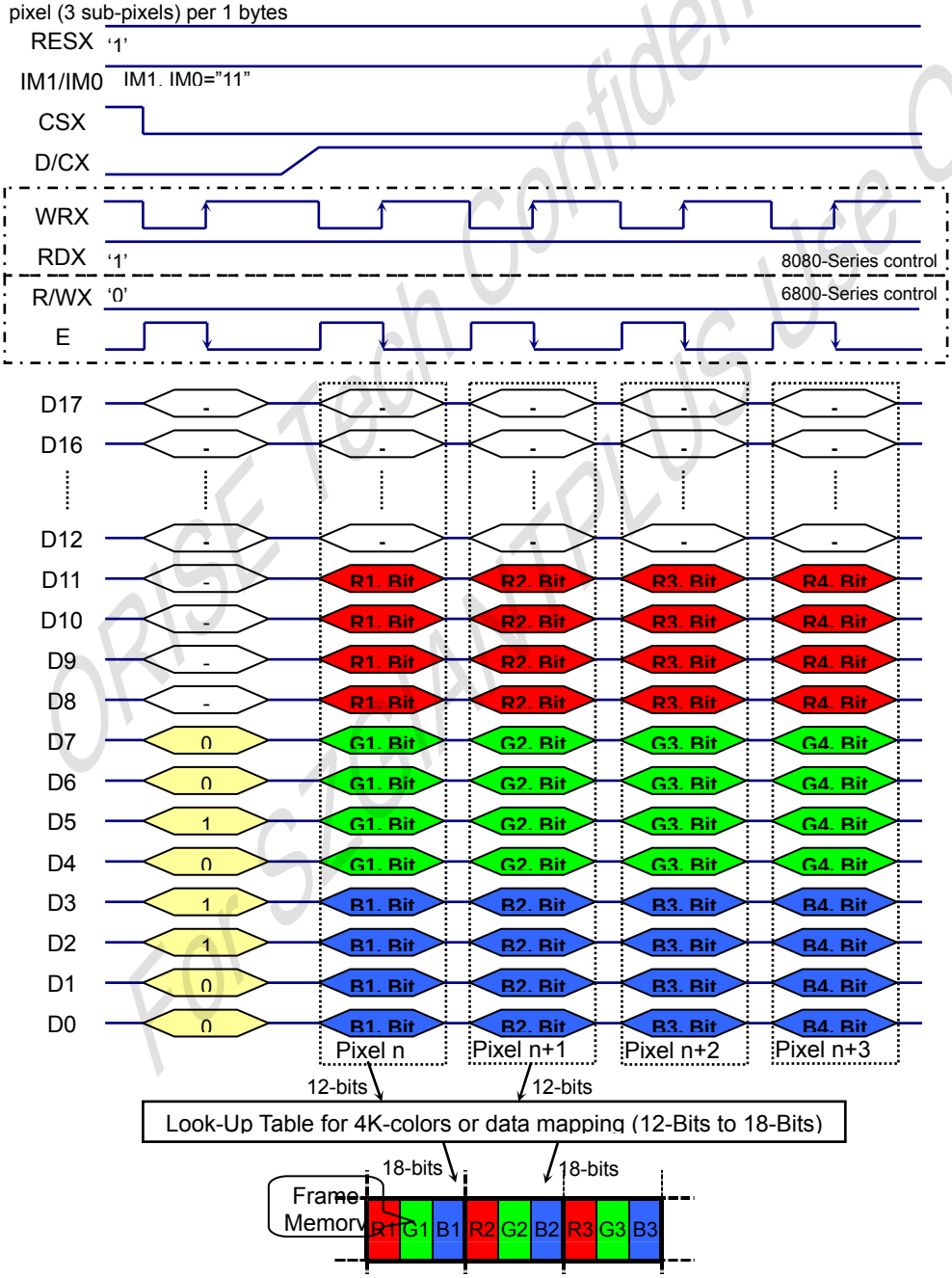
### 7.2.1.4. Parallel 18-Bits Bus Interface for RAM Data Write (IM1, IM0="11")

Different display data formats are available for three colors depth supported by listed below.

- 4K-Colours, RGB 4,4,4-bits input data. (3AH="03h")
- 65K-Colours, RGB 5,6,5-bits input data. (3AH="05h")
- 262K-Colours, RGB 6,6,6-bits input data. (3AH="06h")

(1). 18-bits data bus for 12-bits/pixel (RGB 4-4-4-bits input), 4K-colours, 3AH="03h"

There is 1 pixel (3 sub-pixels) per 1 bytes



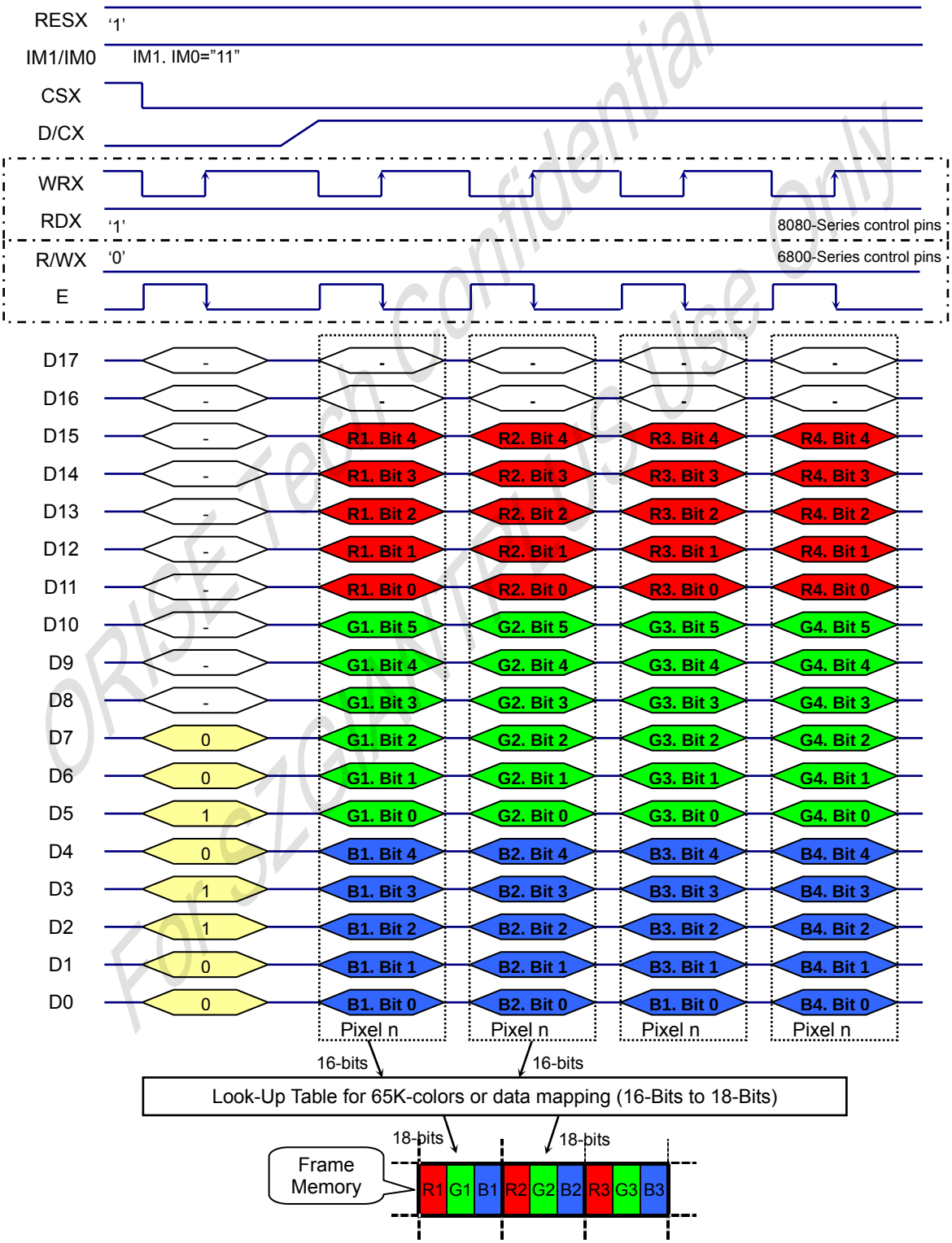

*Note1. The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.*

*Note 2.1-times transfer is used to transmit 1 pixel data with the 12-bits color depth information.*

*Note 3. '-' = Don't care - Can be set to VDDIO or VSS level*

(2). 18-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colours, 3AH="05h"

There are 1 pixel (3 sub-pixels) per 1 bytes



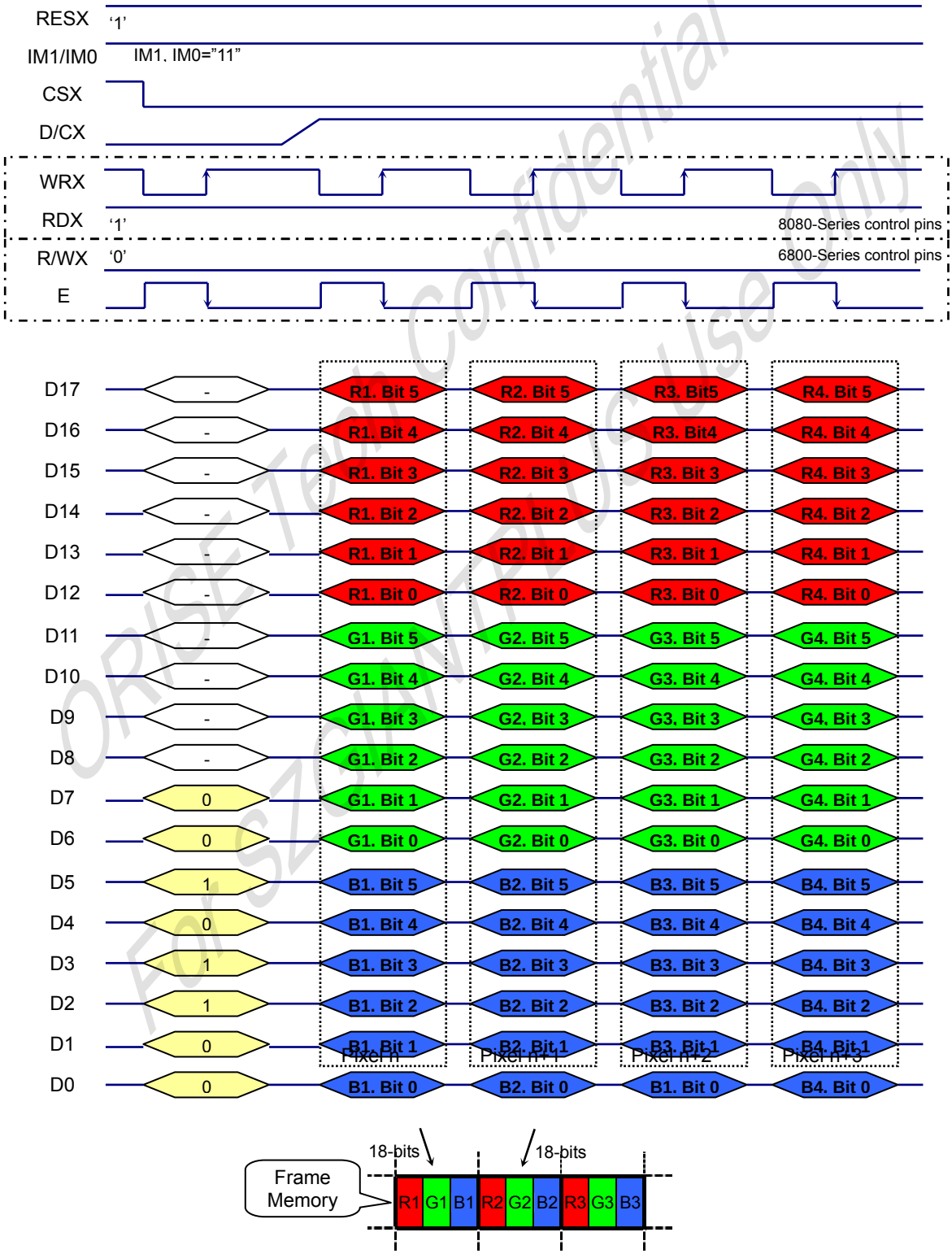

*Note1. The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.*

*Note 2.1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.*

*Note 3. '-' = Don't care - Can be set to VDDIO or VSS level*

(3). 18-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colours, 3AH="06h"

There are 1 pixel (6 sub-pixels) per 1 bytes




*Note1. The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.*

*Note 2.1-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.*

*Note 3. '-' = Don't care - Can be set to VDDIO or VSS level*

### 7.2.2. MCU Data Colour Coding for RAM data ***Read***

- Parallel 8-Bits Bus Interface (IM1, IM0= "00")

Table 7.3.2.1 8-Bits Parallel Interface Set Table

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command |
| | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | **2EH** |
| Read Data Format | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Colour |
| | x | x | x | x | x | x | x | x | x | x | R5 | R4 | R3 | R2 | R1 | R0 | x | x | 262K-Colour (1-pixels/ 3byyes) |
| | x | x | x | x | x | x | x | x | x | x | G5 | G4 | G3 | G2 | G1 | G0 | x | x | |
| | x | x | x | x | x | x | x | x | x | x | B5 | B4 | B3 | B2 | B1 | B0 | x | x | |

- Parallel 16-Bits Bus Interface (IM1, IM0= "10")

Table 7.3.2.2 16-Bits Parallel Interface Set Table

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command |
| | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | **2EH** |
| Read Data Format | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Colour |
| | x | x | R5 | R4 | R3 | R2 | R1 | R0 | x | x | G5 | G4 | G3 | G2 | G1 | G0 | x | x | 262K-Colour (2-pixels/ 3byyes) |
| | x | x | B5 | B4 | B3 | B2 | B1 | B0 | x | x | R5 | R4 | R3 | R2 | R1 | R0 | x | x | |
| | x | x | G5 | G4 | G3 | G2 | G1 | G0 | x | x | B5 | B4 | B3 | B2 | B1 | B0 | x | x | |

- Parallel 9-Bits Parallel Interface (IM1, IM0= "01")

Table 7.3.2.3 9-Bits Parallel Interface Set Table

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register Command | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Register |
| | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | **2EH** |
| Read Data Format | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Colour |
| | x | x | x | x | x | x | x | x | x | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | 262K-Colour (1-pixels/ 2bytes) |
| | x | x | x | x | x | x | x | x | x | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 | |

- Parallel 18-Bits Parallel Interface (IM1, IM0= "11")

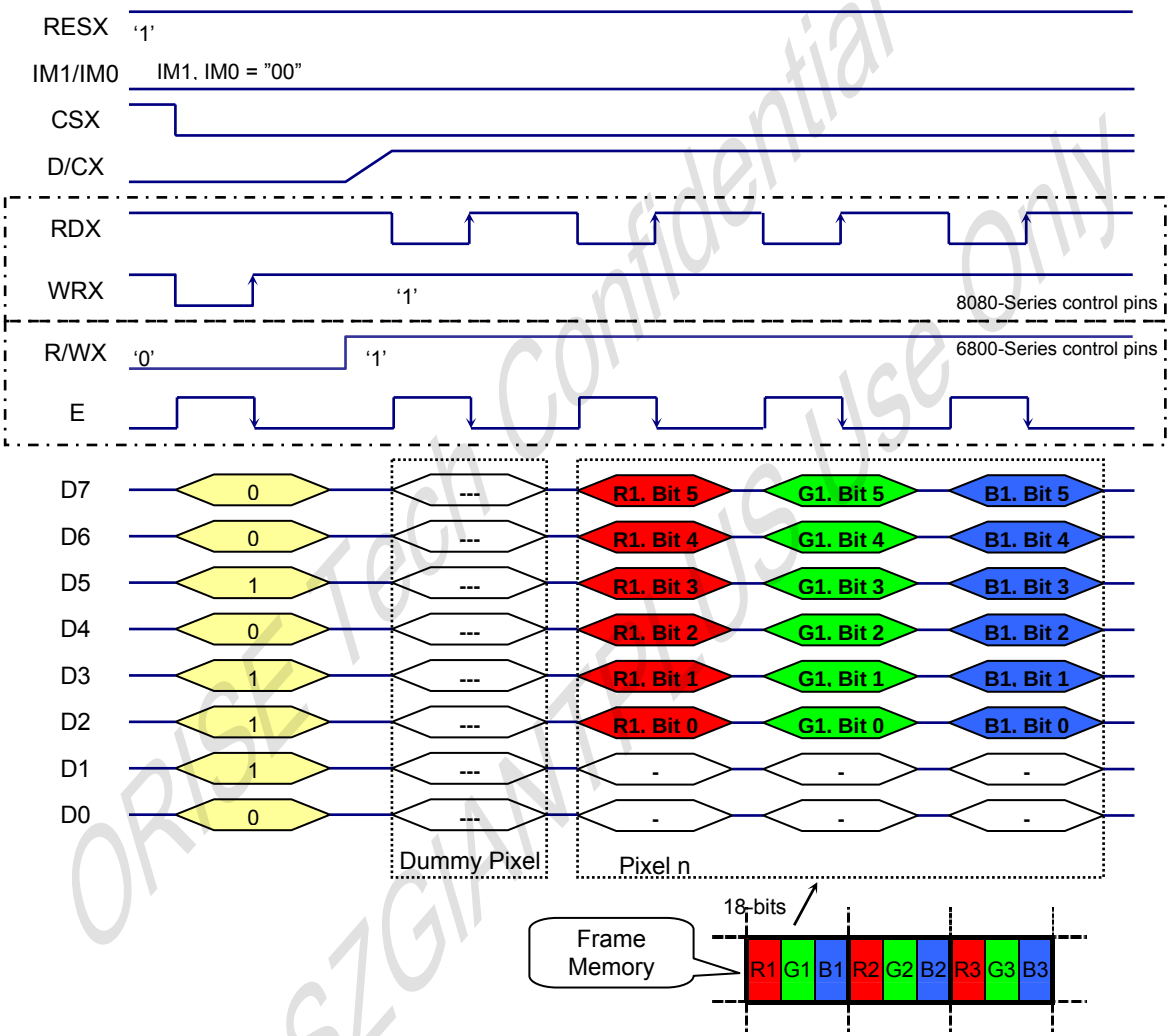
Table 7.3.2.4 18-Bits Parallel Interface Set Table

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Register Command** | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Register |
| | x | x | x | x | x | x | x | x | x | x | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | **2EH** |
| Read Data Format | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 | **262K-Colour** |

*Note . 'x' Don't care, but need to set VDDIO or VSS level.*

#### 7.2.2.1. Parallel 8-Bits Bus Interface for RAM Data Read (IM1, IM0= “00”)

There are 1 pixels (3 sub-pixels) per 3-bytes. (RGB 6-6-6-bits output)



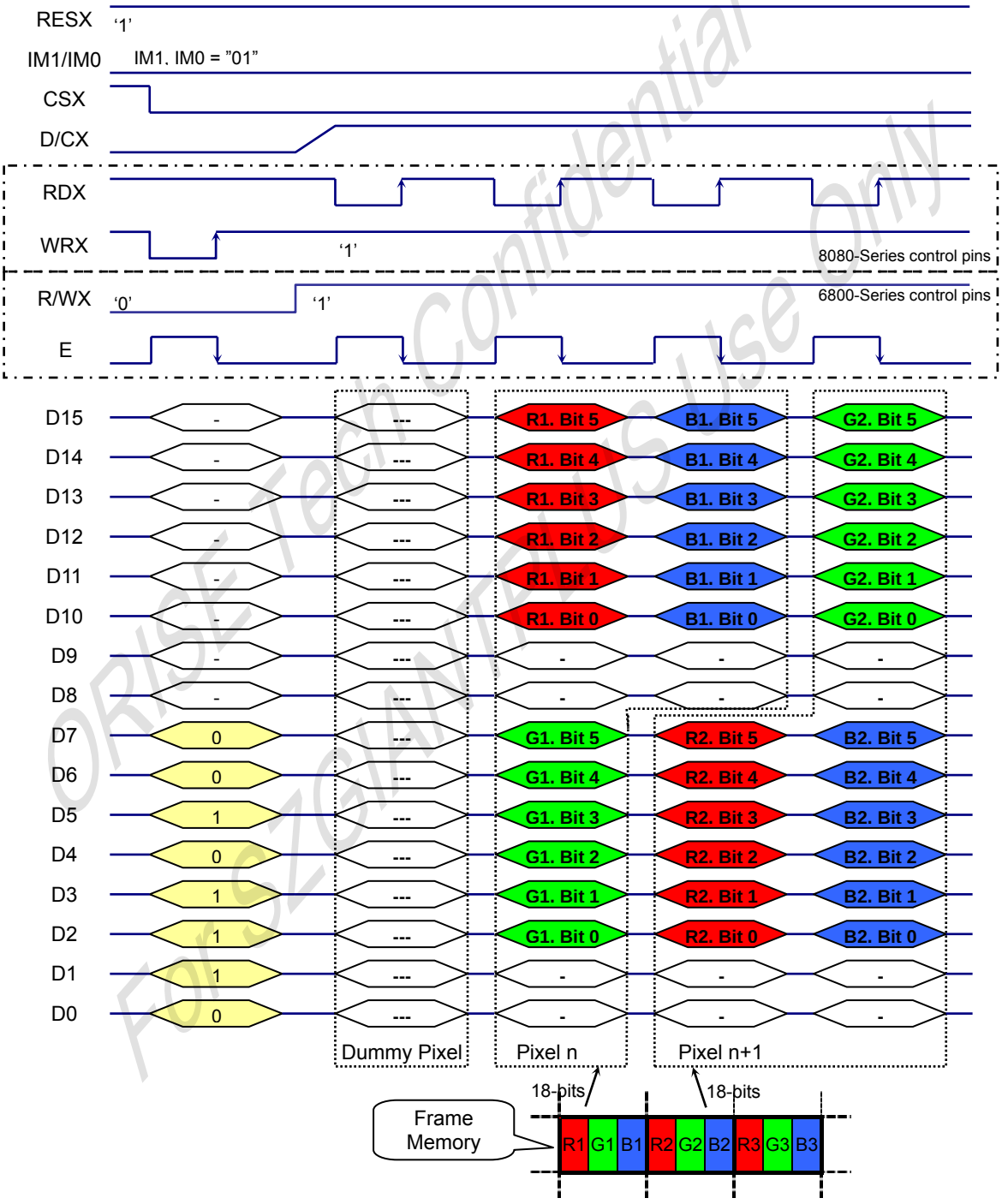

*Note1. The data order is ad follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.*

*Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.*

*Note 3. '-' = Don't care - Can be set to VDDIO or VSS level*

### 7.2.2.2. Parallel 16-Bits Bus Interface for RAM Data Read (IM1, IM0= “10”)

There are 2 pixel (6 sub-pixels) per 3 bytes (RGB 6-6-6-bits output)



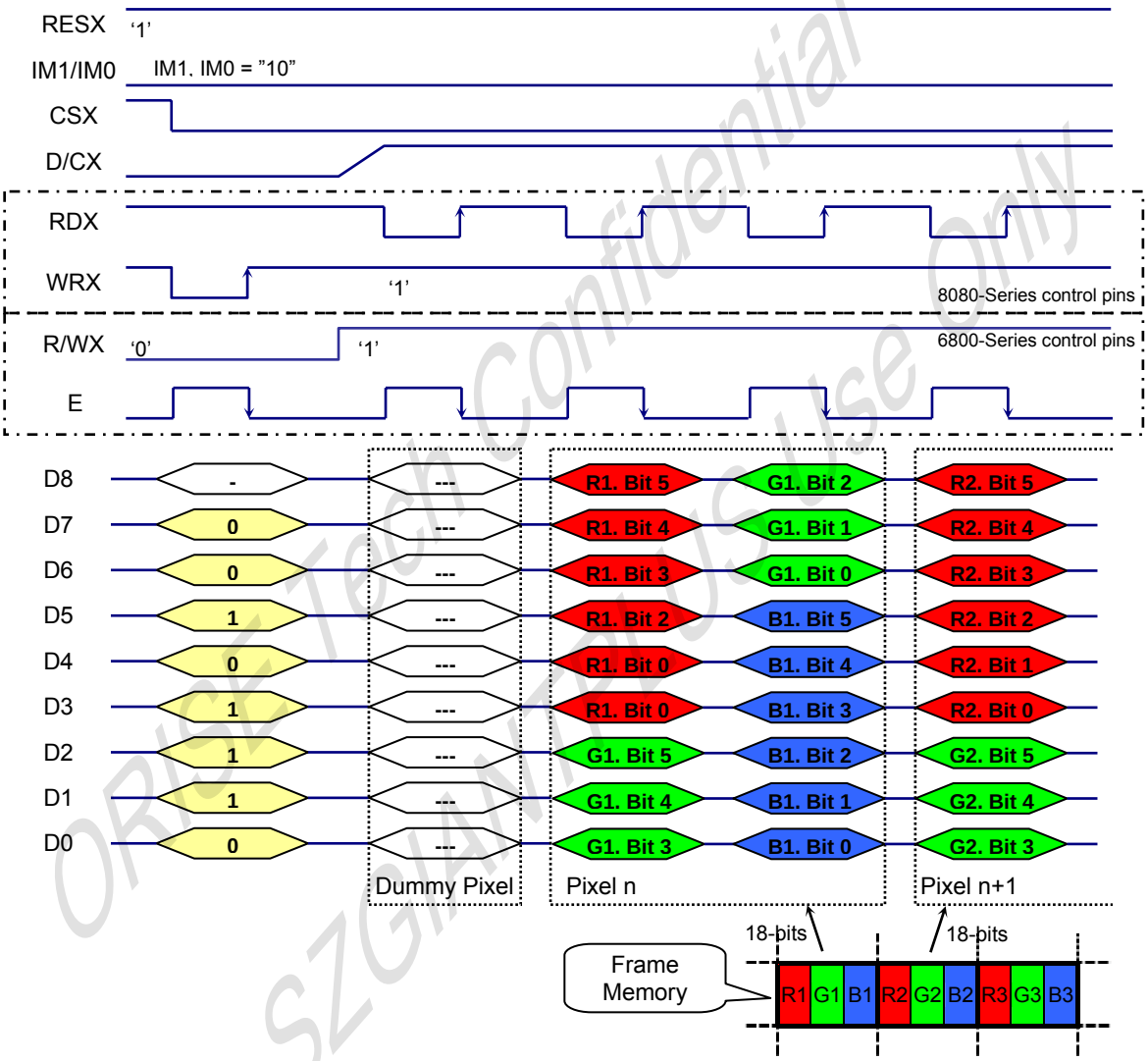

*Note1. The data order is ad follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.*

*Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.*

*Note 3. '-' = Don't care - Can be set to VDDIO or VSS level*

### 7.2.2.3. Parallel 9-Bits Bus Interface for RAM Data Read (IM1, IM0= “01”)

There are 1 pixel (3 sub-pixels) per 2 bytes (RGB 6-6-6-bits output)



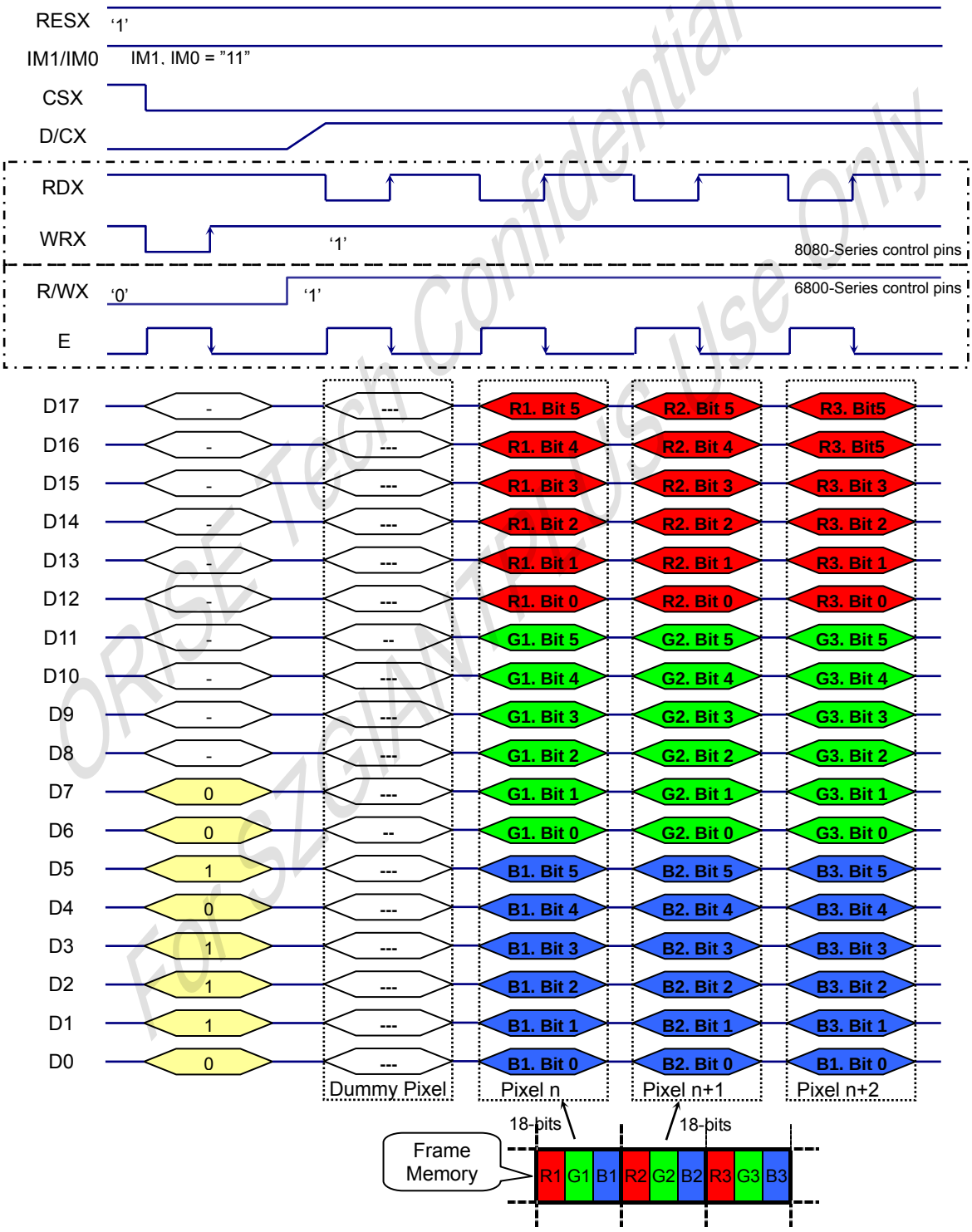

*Note1. The data order is ad follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.*

*Note 2.3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.*

*Note 3. '-' = Don't care - Can be set to VDDIO or VSS level*

### 7.2.2.4. Parallel 18-Bits Bus Interface for RAM Data Read (IM1, IM0= “11”)

There are 1 pixel (3 sub-pixels) per 1 bytes (RGB 6-6-6-bits output)




*Note1. The data order is ad follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.*

*Note 2.1-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.*

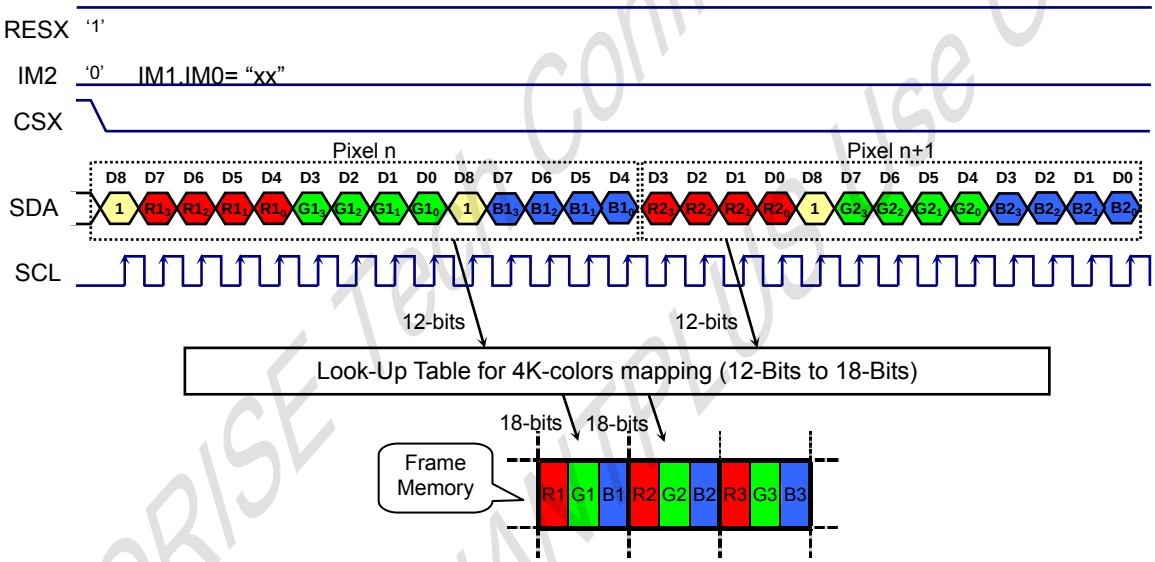
*Note 3. '-' = Don't care - Can be set to VDDIO or VSS level*

### 7.2.3. Serial Interface (IM3 = '1')

Different display data formats are available for three colors depth supported by the LCM listed below.

- 4K-Colours, RGB 4,4,4-bits input data. (3AH="03h")
- 65K-Colours, RGB 5,6,5-bits input data. (3AH="05h")
- 262K-Colours, RGB 6,6,6-bits input data. (3AH="06h")

#### 7.2.3.1. Write data for 12-bits/pixel (RGB 4-4-4-bits input), 4K-colours, 3AH="03h"



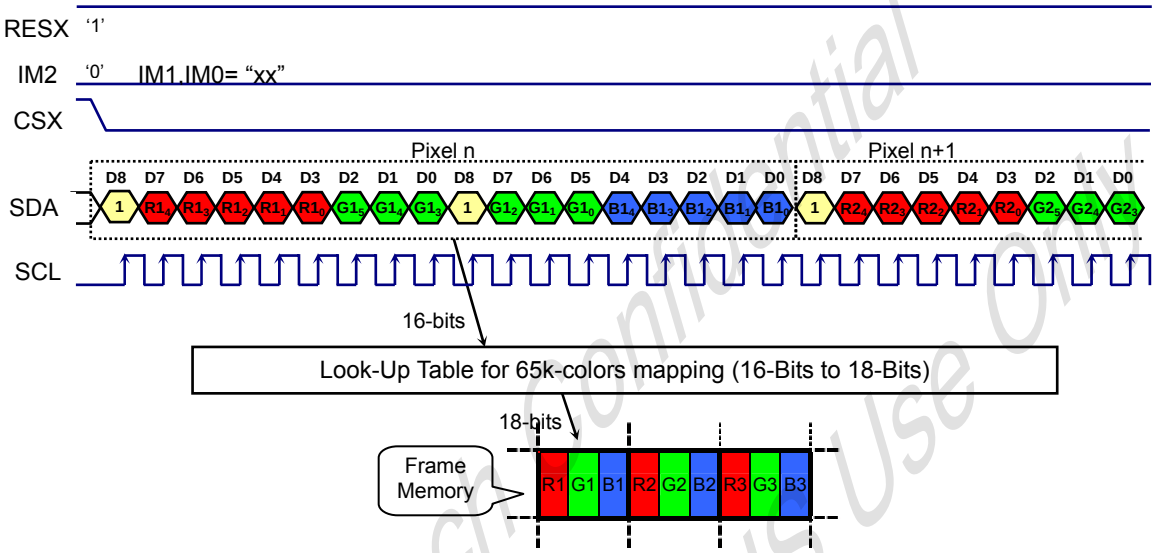

*Note 1. pixel data with the 12-bits color depth information*

*Note 2. The most significant bits are: $Rx_3$, $Gx_3$ and $Bx_3$*

*Note 3. The least significant bits are: $Rx_0$, $Gx_0$ and $Bx_0$*

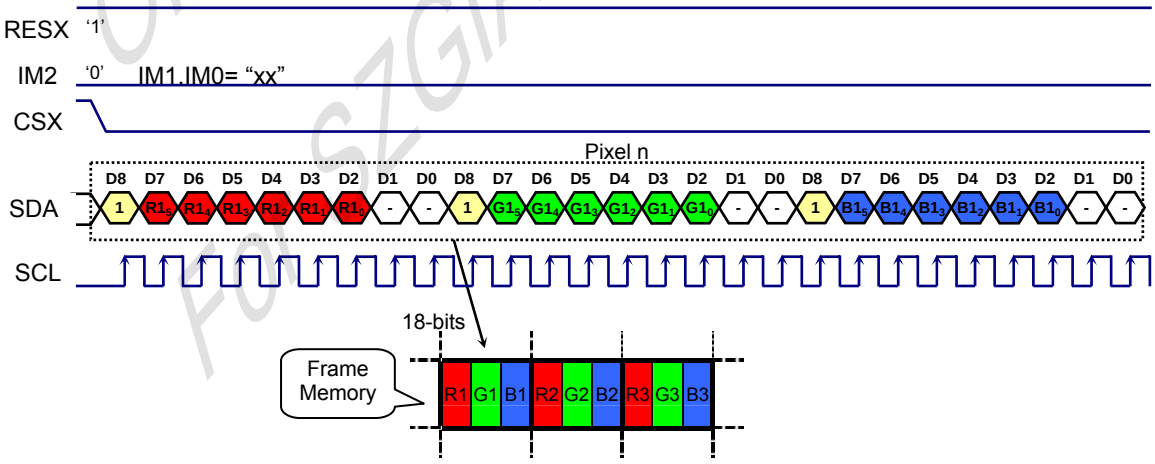
*Note 4. '-' = Don't care - Can be set to VDDIO or VSS level*

### 7.2.3.2. Write data for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colours, 3AH="05h"




*Note 1. pixel data with the 16-bits color depth information*
*Note 2. The most significant bits are: $Rx_4$, $Gx_5$ and $Bx_4$*
*Note 3. The least significant bits are: $Rx_0$, $Gx_0$ and $Bx_0$*
*Note 4. '-' = Don't care - Can be set to VDDIO or VSS level*

### 7.2.3.3. Write data for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colours, 3AH="06h"




*Note 1. pixel data with the 18-bits color depth information*
*Note 2. The most significant bits are: $Rx_5$, $Gx_5$ and $Bx_5$*
*Note 3. The least significant bits are: $Rx_0$, $Gx_0$ and $Bx_0$*
*Note 4. '-' = Don't care - Can be set to VDDIO or VSS level*

### 7.3. Display Data RAM

#### 7.3.1. Configuration

The display module has an integrated 240x320x18-bit graphic type static RAM. This 1,382,400-bits memory allows to store on-chip a 240xRGBx320 image with an 18-bpp resolution (262K-color).

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read

and interface Read or Write to the same location of the Frame Memory.

Display Data RAM Organization

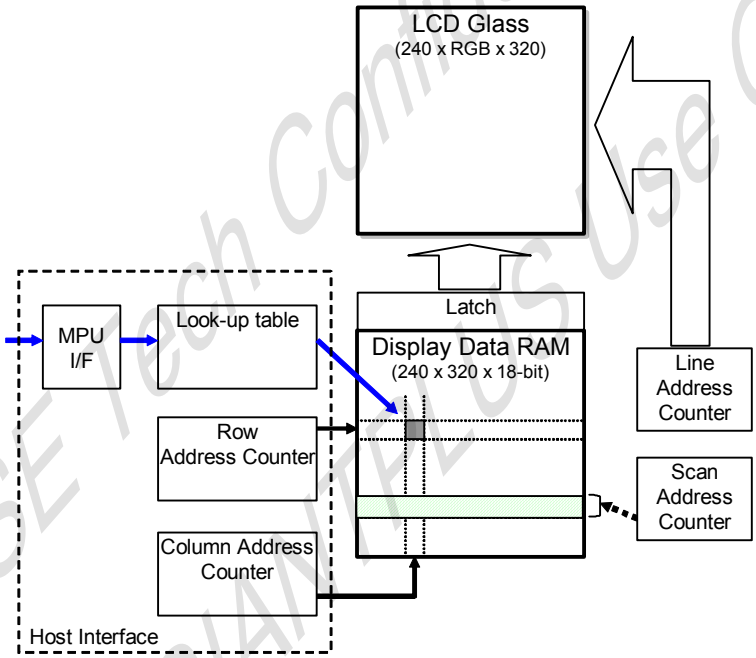
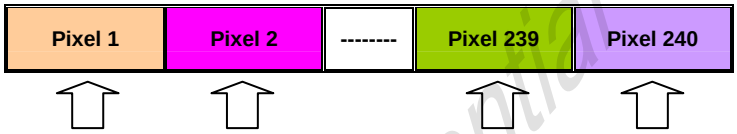



Fig. 7.5.1.1 Display Date RAM Organization

### 7.3.2. Memory to Display Address Mapping

#### 7.3.2.1. When using 240RGB x 320 resolution (SMX=SMY=SRGB='0')




| Gate Out | Source Out | | S1 | S2 | S3 | S4 | S5 | S6 | -------- | S715 | S716 | S717 | S718 | S719 | S720 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RA | | RGB=0 / RGB=1 | | | RGB=0 / RGB=1 | | | RGB Order | RGB=0 / RGB=1 | | | RGB=0 / RGB=1 | | | SA | |
| | MY='0' | MY='1' | | | | | | | | | | | | | | ML='0' | ML='1' |
| **1** | 0 | 319 | R0 | G0 | B0 | R1 | G1 | B1 | -------- | R238 | G238 | B238 | R239 | G239 | B239 | 0 | 319 |
| **2** | 1 | 318 | | | | | | | -------- | | | | | | | 1 | 318 |
| **3** | 2 | 317 | | | | | | | -------- | | | | | | | 2 | 317 |
| **4** | 3 | 316 | | | | | | | -------- | | | | | | | 3 | 316 |
| **5** | 4 | 315 | | | | | | | -------- | | | | | | | 4 | 315 |
| **6** | 5 | 314 | | | | | | | -------- | | | | | | | 5 | 314 |
| **7** | 6 | 313 | | | | | | | -------- | | | | | | | 6 | 313 |
| **8** | 7 | 312 | | | | | | | -------- | | | | | | | 7 | 312 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| **313** | 312 | 7 | | | | | | | -------- | | | | | | | 312 | 7 |
| **314** | 313 | 6 | | | | | | | -------- | | | | | | | 313 | 6 |
| **315** | 314 | 5 | | | | | | | -------- | | | | | | | 314 | 5 |
| **316** | 315 | 4 | | | | | | | -------- | | | | | | | 315 | 4 |
| **317** | 316 | 3 | | | | | | | -------- | | | | | | | 316 | 3 |
| **318** | 317 | 2 | | | | | | | -------- | | | | | | | 317 | 2 |
| **319** | 318 | 1 | | | | | | | -------- | | | | | | | 318 | 1 |
| **320** | 319 | 0 | | | | | | | -------- | | | | | | | 319 | 0 |
| | CA | MX='0' | 0 | | | 1 | | | -------- | 238 | | | 239 | | | | |
| | | MX='1' | 239 | | | 238 | | | -------- | 1 | | | 0 | | | | |

*Note*

*RA = Row Address,*

*CA = Column Address*

*SA = Scan Address*

*MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command*

*MY = Mirror Y-axis (Column address direction parameter), D7 parameter of MADCTL command*

*MX =Scan direction parameter, D4 parameter of MADCTL command*

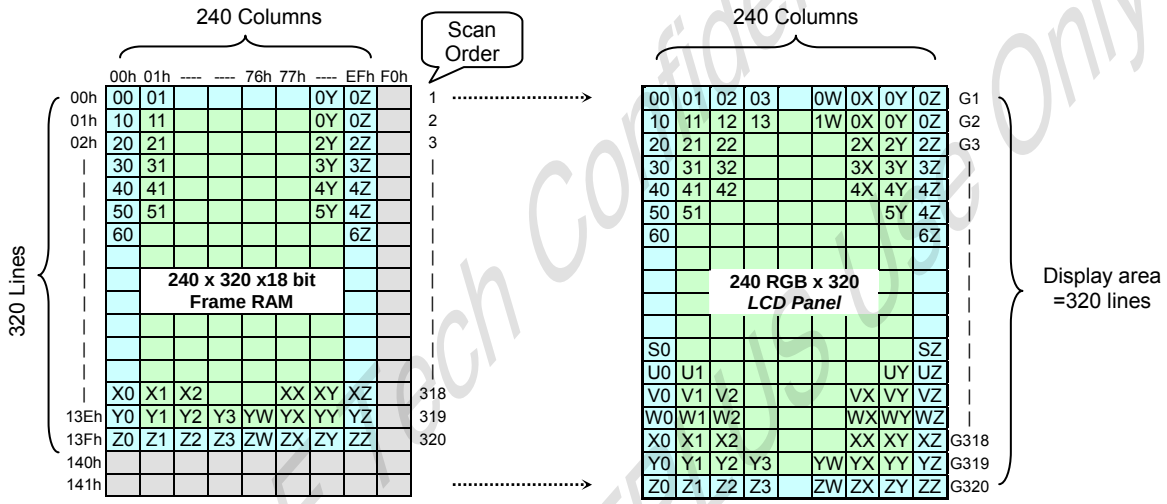
*RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command*

### 7.3.3. Normal Display On or Partial Mode On, Vertical Scroll Off

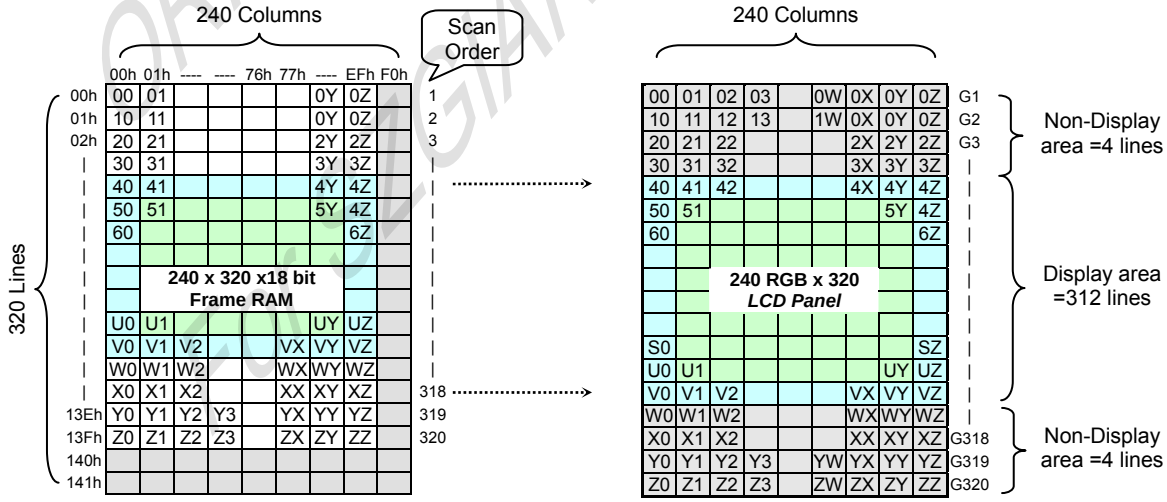
#### 7.3.3.1. When using 240RGB x 320 resolution

In this mode, contents of the frame memory within an area where column pointer is 00h to EFh and page pointer is 00h to 13Fh is displayed.To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

(1) Example for Normal Display On (MX=MY=ML='0' ,SMX=SMY='0')




(2). Example for Partial Display On (PSL[7:0]=04h,PEL[7:0]=13Bh, MX=MV=ML='0' ,SMX=SMY='0')



### 7.3.4. Vertical Scroll Mode

There is vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

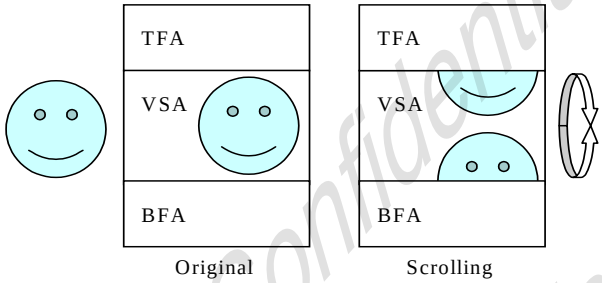
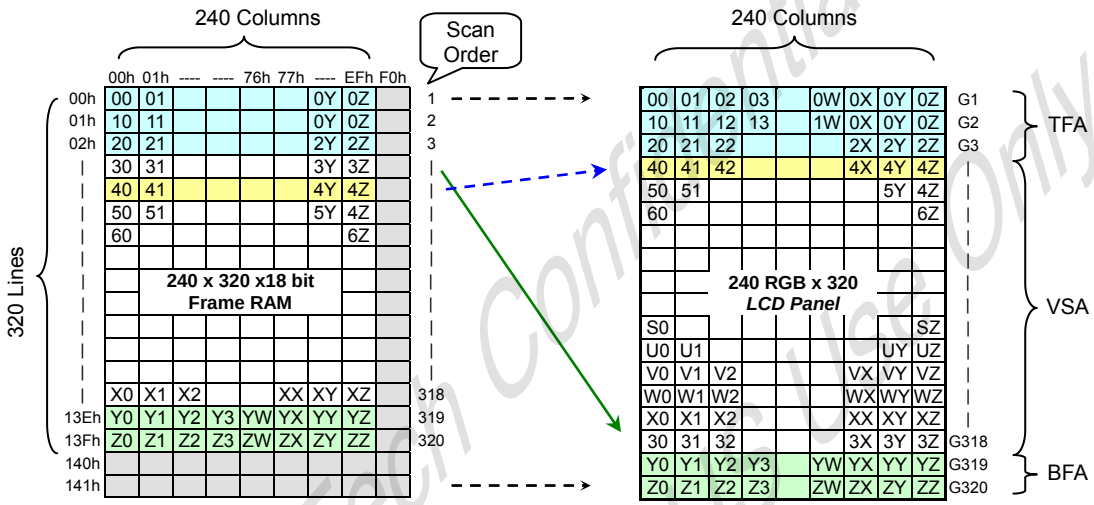



Fig. 7.5.4.1 Difference between Scrolling and original

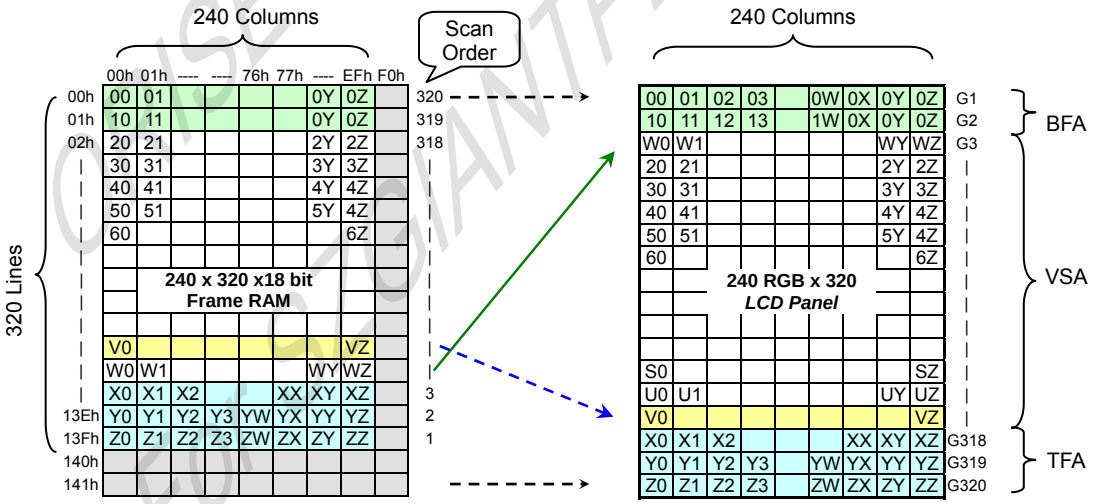
### 7.3.4.1. When using 240RGB x 320 resolution

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=320. In this case, scrolling is applied as shown below.

(1) Example for TFA =3, VSA=315, BFA=2, SSA=4, ML=0: Scrolling




(2) Example for TFA =3, VSA=315, BFA=2, SSA=4, ML=1: Scrolling: TFA and BFT are exchanged



### 7.3.5. Vertical Scroll Example

#### 7.3.5.1. Vertical Scroll Example

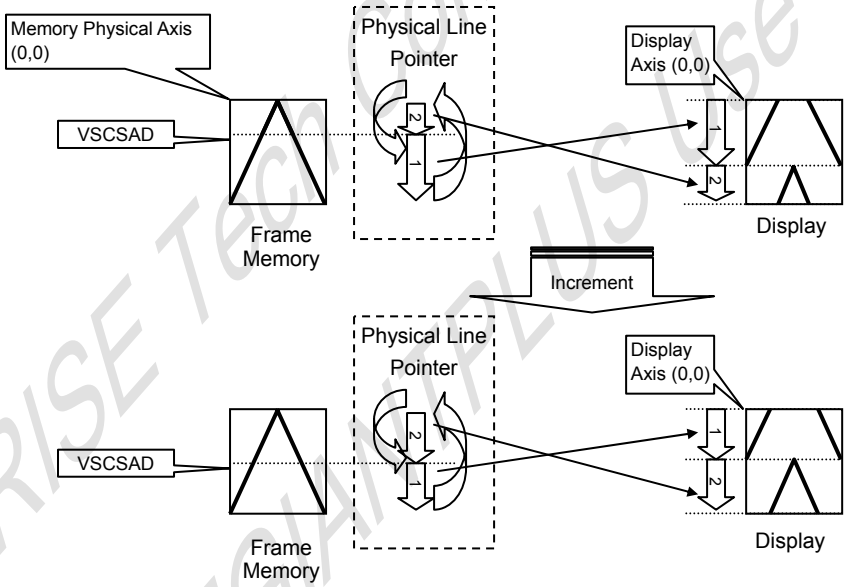
There are 2 types of vertical scrolling, which are determined by the commands " Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

**Case 1: TFA + VSA + BFA≠320**

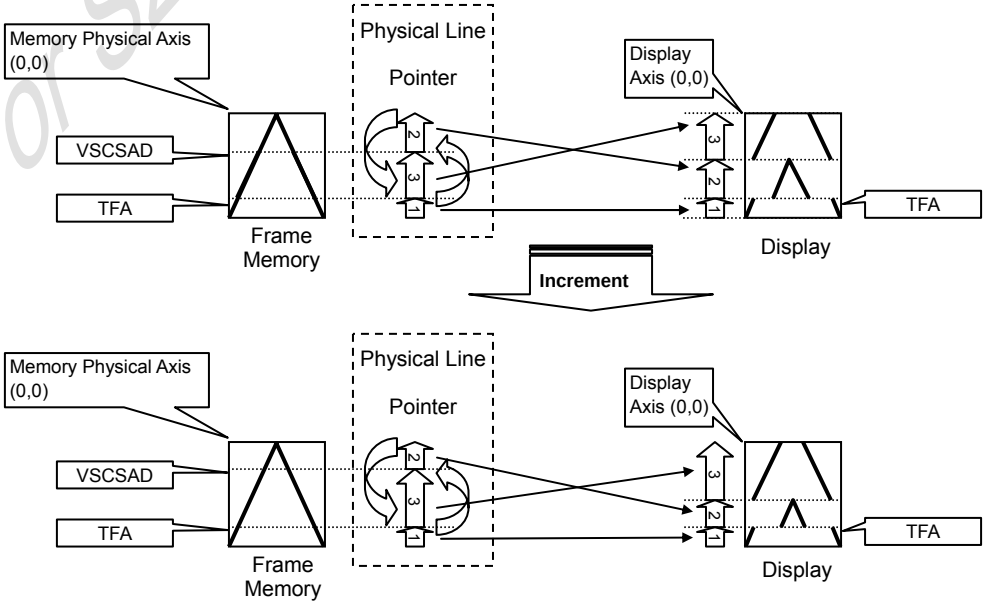
N/A. Do not set TFA + VSA + BFA≠320. In that case, unexpected picture will be shown.

**Case 2: TFA + VSA + BFA=320 (Scrolling)**

Example1) When MADCTR parameter ML="0", TFA=0, VSA=320, BFA=0 and VSCSAD=160.




Example2) When MADCTR parameter ML="1", TFA=60, VSA=260, BFA=0 and VSCSAD=160.



### 7.4. Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 8-8-8-bit), according to the data formats. As soon as this pixel-data information is complete the “Write access” is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=240 (EFh) and Y=0 to Y=320 (13Fh). Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined into which will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=240 (EFh), YE=320 (13Fh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

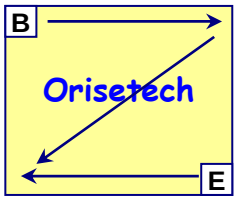
For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET” and “MADCTR” , define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Fig. 8.2.3 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as Fig. 7.6.1 below:

| Condition | Column Counter | Row Counter |
|---|---|---|
| When RAMWR/RAMRD command is accepted | Return to “Start Column (XS)” | Return to “Start Row (YS)” |
| Complete Pixel Read / Write action | Increment by 1 | No change |
| The Column counter value is larger than “End Column (XE)” | Return to “Start Column (XS)” | Increment by 1 |
| The Column counter value is larger than “End Column (XE)” and the Row counter value is larger than “End Row (YE)” | Return to “Start Column (XS)” | Return to “Start Row (YS)” |

### 7.5. Memory Data Write/ Read Direction

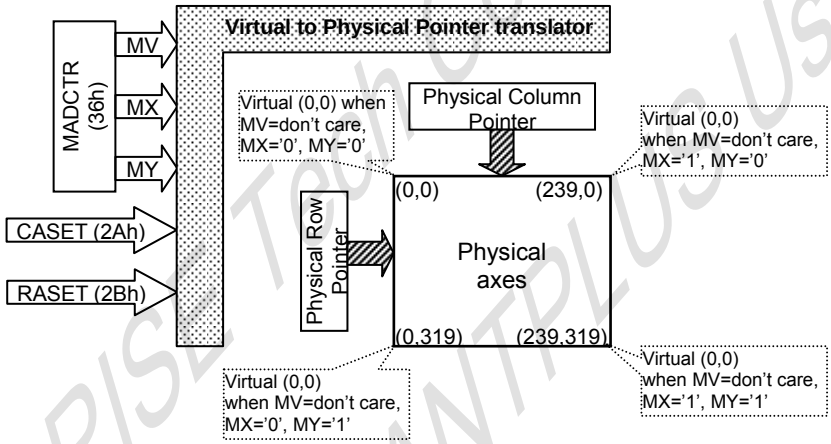
The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, bits B5 (MV), B6 (MX), B7 (MY) as described below.




Data Stream order is like in this figure

Fig. 7.7.1 Data streaming order

-When 240RGBx320

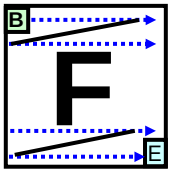
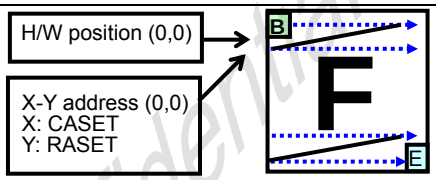
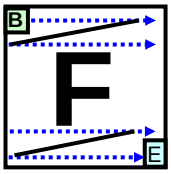
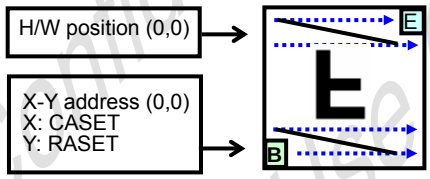
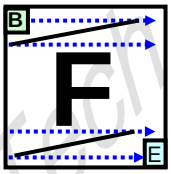
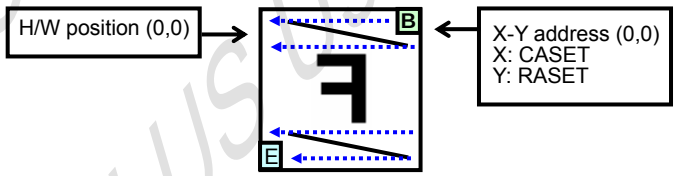
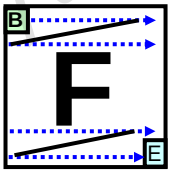
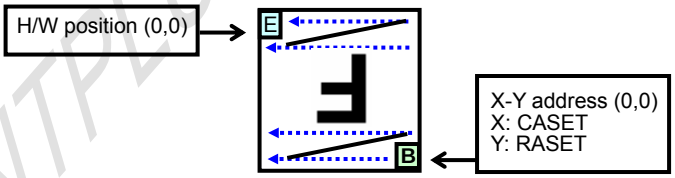
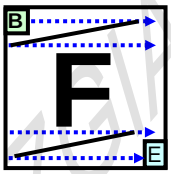
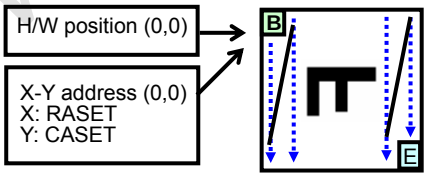
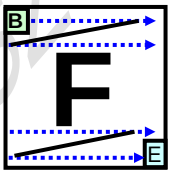
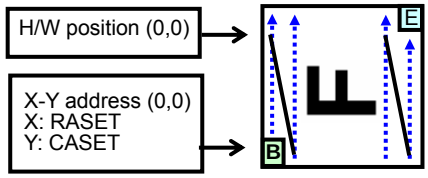
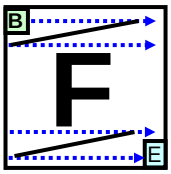
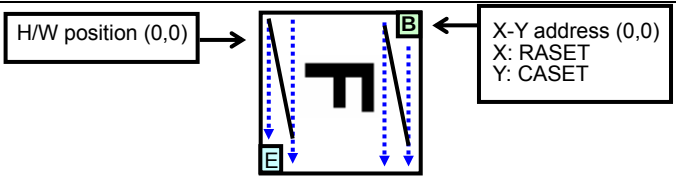
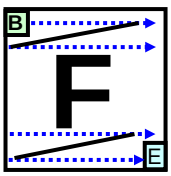
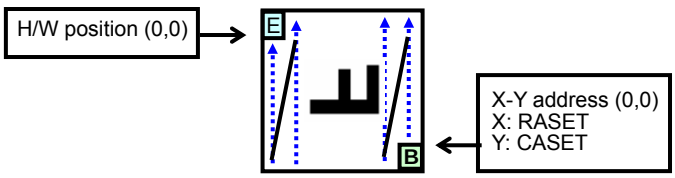



| MV | MX | MV | CASET | RASET |
|---|---|---|---|---|
| 0 | 0 | 0 | Direct to Physical Column Pointer | Direct to Physical Row Pointer |
| 0 | 0 | 1 | Direct to Physical Column Pointer | Direct to (319-Physical Row Pointer) |
| 0 | 1 | 0 | Direct to (239-Physical Column Pointer) | Direct to Physical Row Pointer |
| 0 | 1 | 1 | Direct to (239-Physical Column Pointer) | Direct to (319-Physical Row Pointer) |
| 1 | 0 | 0 | Direct to Physical Row Pointer | Direct to Physical Column Pointer |
| 1 | 0 | 1 | Direct to (319-Physical Row Pointer) | Direct to Physical Column Pointer |
| 1 | 1 | 0 | Direct to Physical Row Pointer | Direct to (239-Physical Column Pointer) |
| 1 | 1 | 1 | Direct to (319-Physical Row Pointer) | Direct to (239-Physical Column Pointer) |

*Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7 (MY), B6 (MX), B5 (MV). The write order for each pixel unit is*

| D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 |

Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)

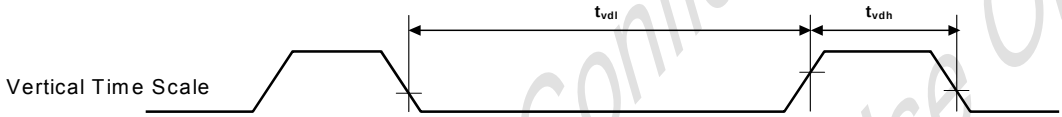
| Display Data Direction | MADCTR Parameter | | | Image in the Host (MPU) | Image in the Driver (DDRAM) |
|---|---|---|---|---|---|
| | MV | MX | MY | | |
| Normal | 0 | 0 | 0 |  |  |
| Y-Mirror | 0 | 0 | 1 |  |  |
| X-Mirror | 0 | 1 | 0 |  |  |
| X-Mirror<br>Y-Mirror | 0 | 1 | 1 |  |  |
| X-Y Exchange | 1 | 0 | 0 |  |  |
| X-Y Exchange<br>Y-Mirror | 1 | 0 | 1 |  |  |
| X-Y Exchange<br>X-Mirror | 1 | 1 | 0 |  |  |
| X-Y Exchange<br>X-Mirror<br>Y-Mirror | 1 | 1 | 1 |  |  |

### 7.6. Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

#### 7.6.1. Tearing Effect Line Modes

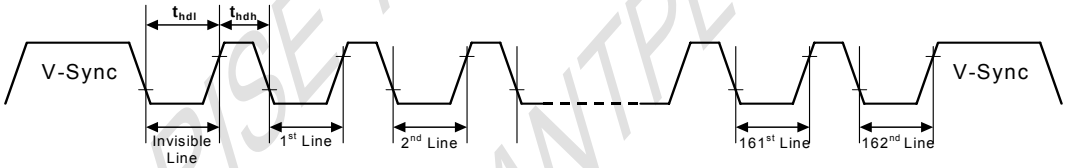
**Mode 1**, the Tearing Effect Output signal consists of V-Blanking Information only:




*$t_{vdh}$= The LCD display is not updated from the Frame Memory*

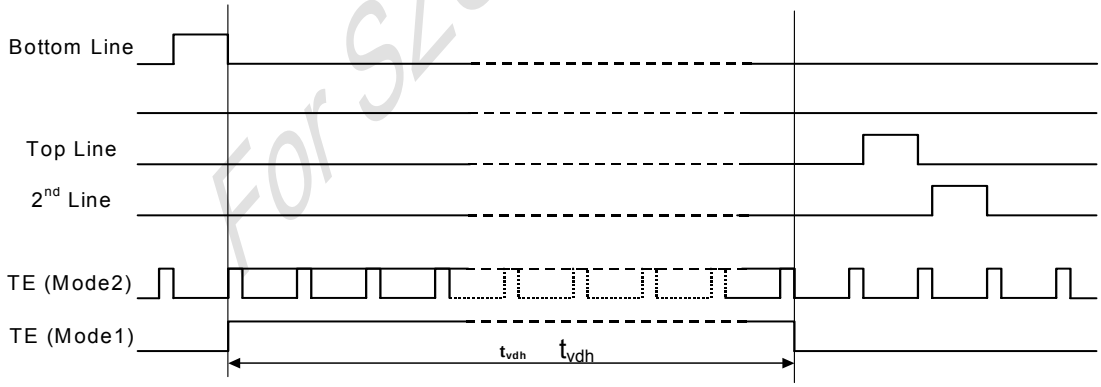
*$t_{vdl}$= The LCD display is updated from the Frame Memory (except Invisible Line – see below)*

**Mode 2**, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 162 H-sync pulses per field.




*$t_{hdh}$= The LCD display is not updated from the Frame Memory*

*$t_{hdl}$= The LCD display is updated from the Frame Memory (except Invisible Line – see above)*




*Note: During Sleep In Mode, the Tearing Output Pin is active Low.*

### 7.6.2. Tearing Effect Line Timings

The Tearing Effect signal is described below:

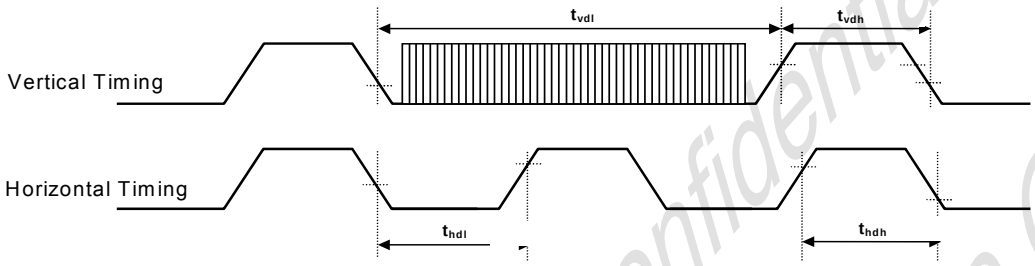



Table 7.8.1 AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 60 Hz)

| Symbol | Parameter | min | max | unit | description |
|---|---|---|---|---|---|
| $t_{vdl}$ | Vertical Timing Low Duration | 13 | 20 | ms | |
| $t_{vdh}$ | Vertical Timing High Duration | 1000 | 1500 | $\mu$s | |
| $t_{hdl}$ | Horizontal Timing Low Duration | 33 | - | $\mu$s | |
| $t_{hdh}$ | Horizontal Timing High Duration | 25 | 500 | $\mu$s | |

*NOTE: The timings in Table 7.8.1 apply when MADCTR ML=0 and ML=1*

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

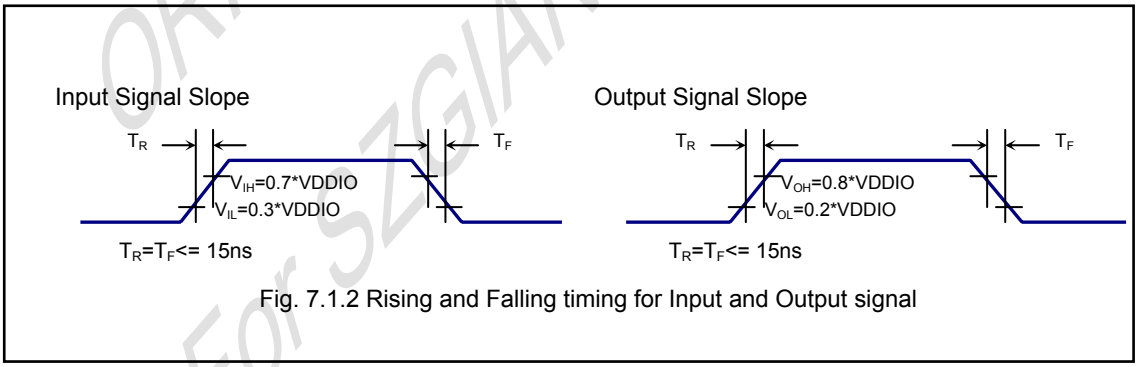
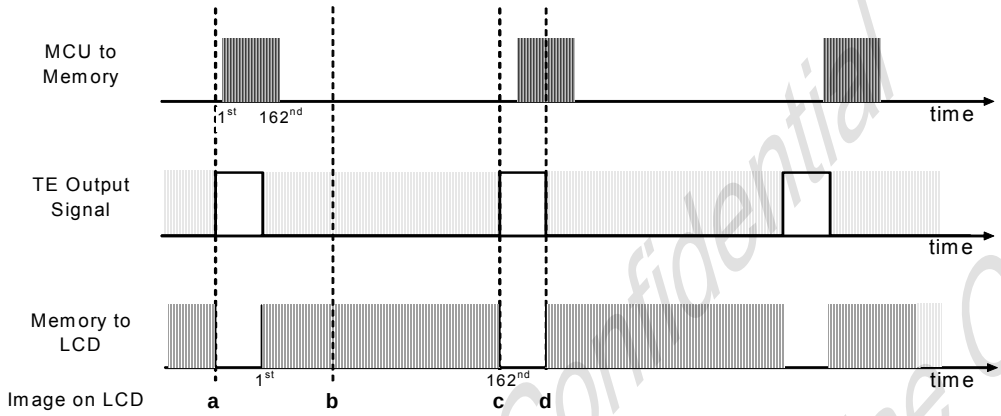


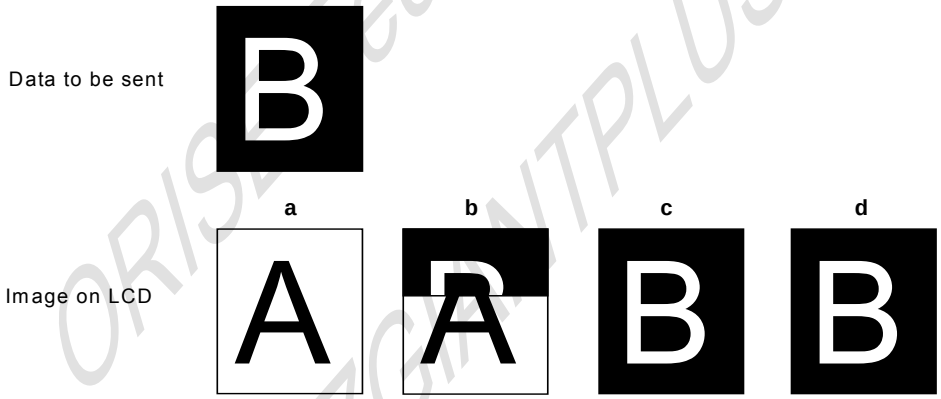

Fig. 7.1.2 Rising and Falling timing for Input and Output signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

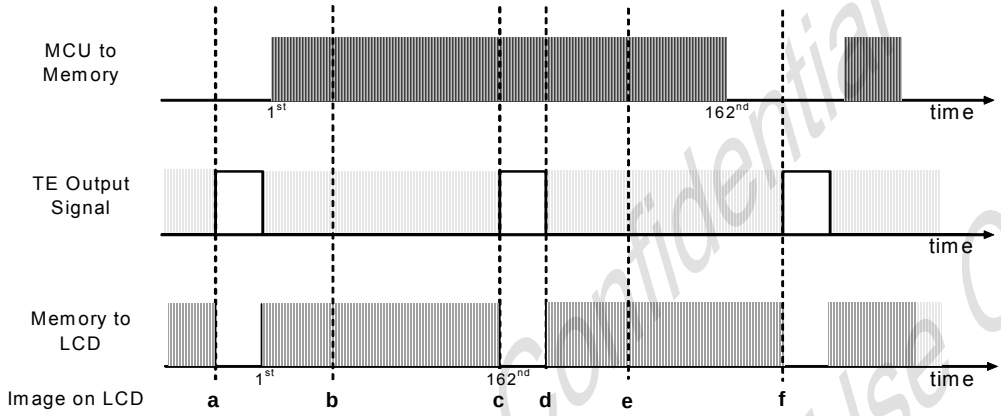
### 7.6.3. Example 1: MPU Write is faster than panel read.



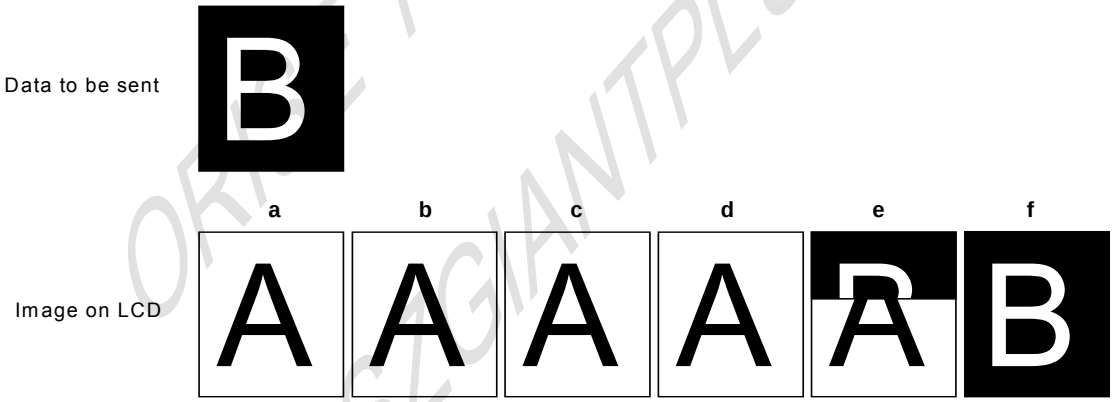

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



### 7.6.4. Example 2: MPU write is slower than panel read.




The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



### 7.7. Preset Values

ORISETECH has already set all preset values in OTM3206A. Any of these preset values do not need customer's SW support.

### 7.8. Power ON/OFF Sequence

VDDIO and VDD can be applied in any order.

VDDIO and VDD can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDIO must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDIO or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

*Note 1: There will be no damage to the display module if the power sequences are not met.*

*Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.*

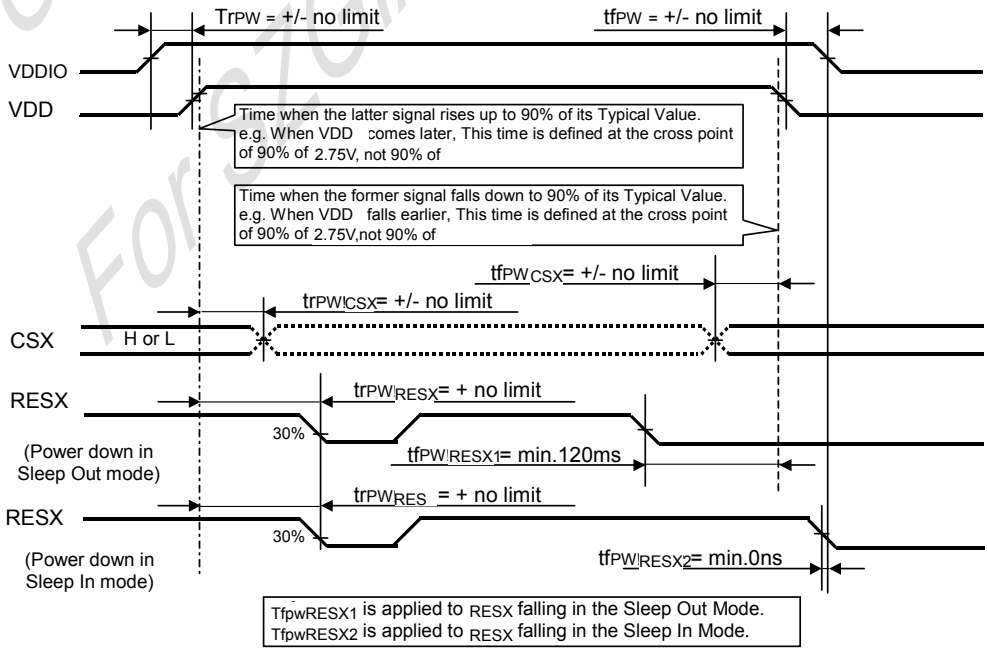
*Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.*

If RESX line is not held stable by host during Power On Sequence, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

#### 7.8.1. Case 1 – RESX Line is held High or Unstable by Host at Power On

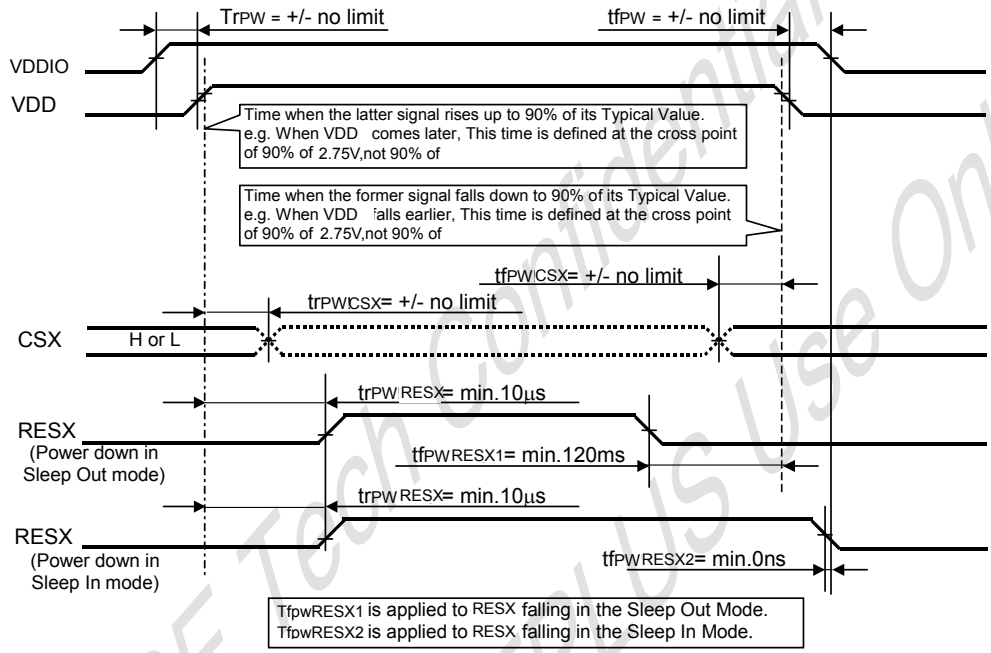
If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD and VDDIO have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.




*Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.*

### 7.8.2. Case 2 – RESX Line is Held Low by Host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10μsec after both VDD and VDDIO have been applied.




*Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.*

### 7.8.3. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface.

At an uncontrolled power off the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

### 7.9. Power Level Definition

#### 7.9.1. Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

**1. Normal Mode On (full display), Idle Mode Off, Sleep Out.**

In this mode, the display is able to show maximum 262,144 colors.

**2. Partial Mode On, Idle Mode Off, Sleep Out.**

In this mode part of the display is used with maximum 262,144 colors.

**3. Normal Mode On (full display), Idle Mode On, Sleep Out.**

In this mode, the full display area is used but with 8 colors.

**4. Partial Mode On, Idle Mode On, Sleep Out.**

In this mode, part of the display is used but with 8 colors.

**5. Sleep In Mode**

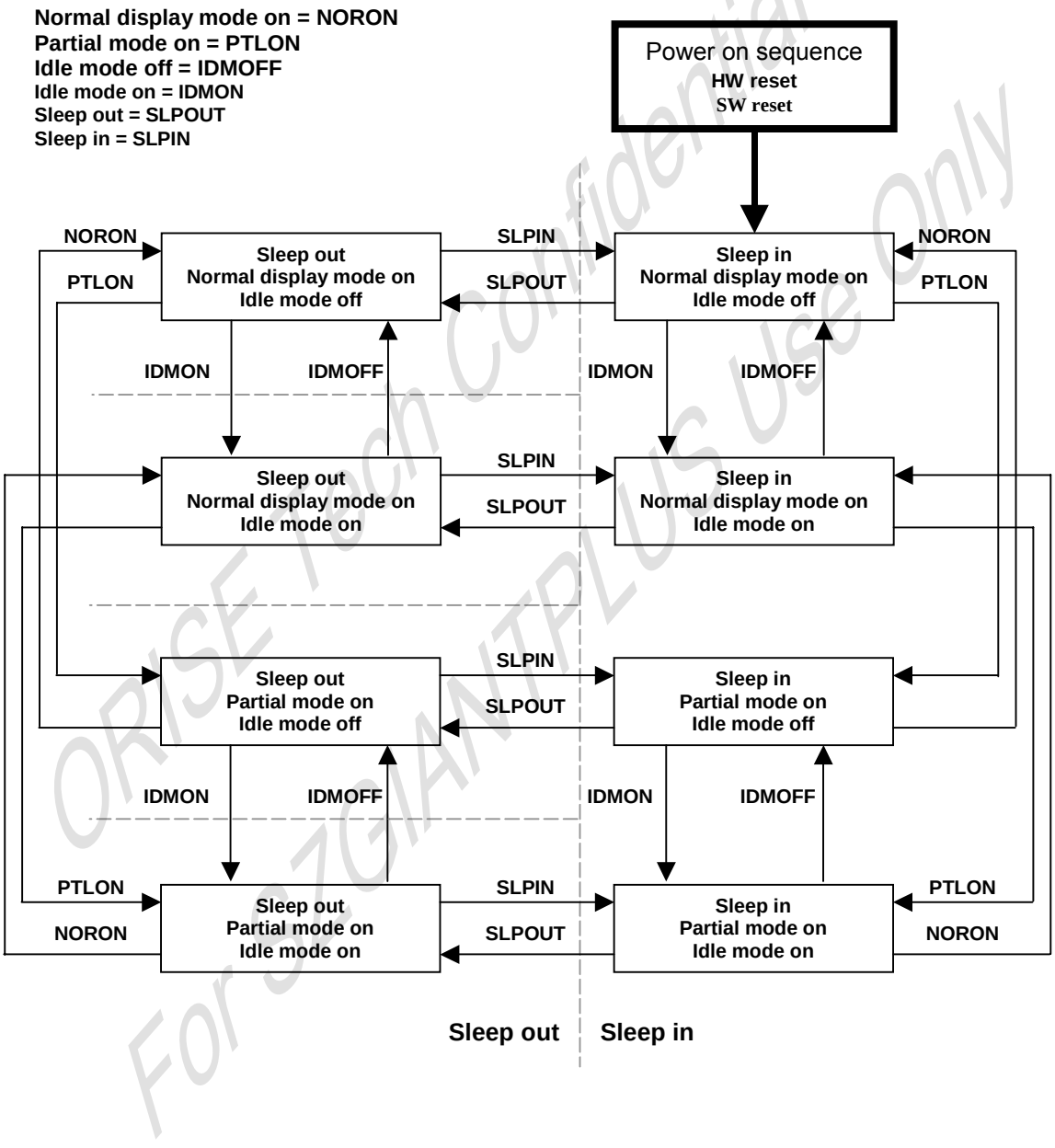
In this mode, the DC: DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDIO power supply. Contents of the memory are safe.

**6. Power Off Mode**

In this mode, both VDD and VDDIO are removed.

*Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.*

### 7.9.2. Power Flow Chart

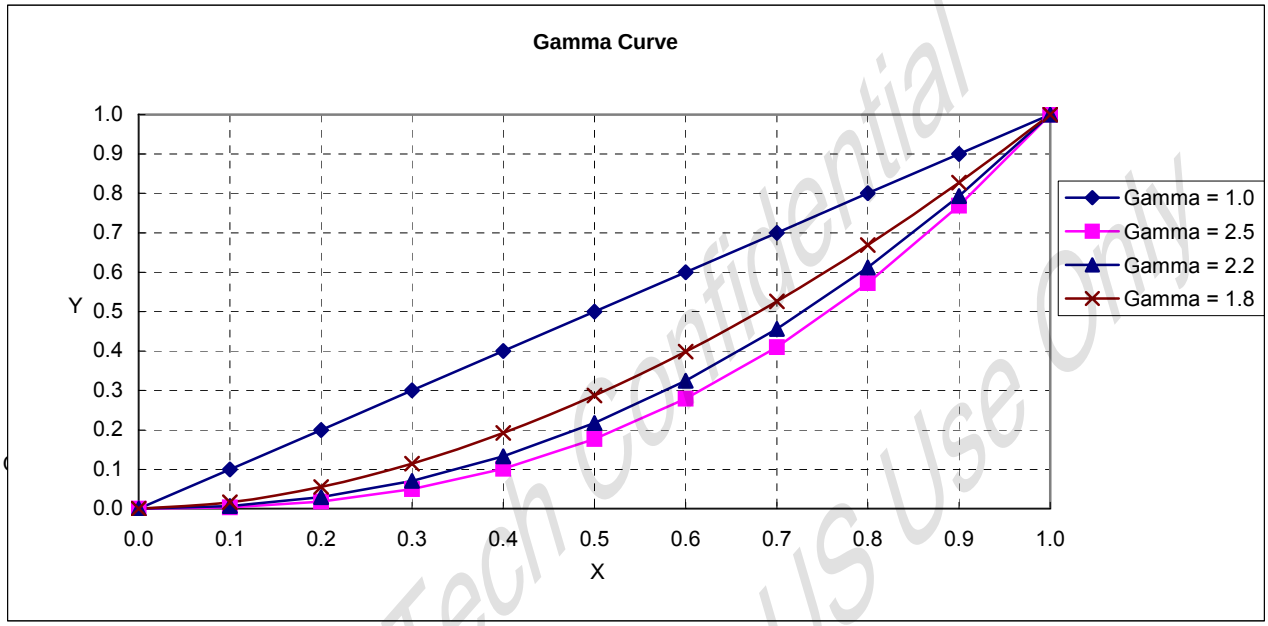





*Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.*

*Note 2: There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode.*

### 7.10. Gamma Curves



### 7.11. Reset

#### 7.11.1. Reset Value

##### 7.11.1.1. Reset Table

| Item | After Power On | After Hardware Reset | After Software Reset |
|---|---|---|---|
| Frame memory | Random | No Change | No Change |
| Sleep In/Out | In | In | In |
| Display On/Off | Off | Off | Off |
| Display mode (normal/partial) | Normal | Normal | Normal |
| Display Inversion On/Off | Off | Off | Off |
| Display Idle Mode On/Off | Off | Off | Off |
| Column: Start Address (XS) | 0000h | 0000h | 0000h |
| Column: End Address (XE) | 00EFh | 00EFh | 00EFh (239d)(when MV=0)<br>013Fh (319d)(when MV=1) |
| Row: Start Address (YS) | 0000h | 0000h | 0000h |
| Row: End Address (YE) | 013Fh | 013Fh | 013Fh (319d)(when MV=0)<br>00EFh (127d)(when MV=1) |
| Gamma setting | GC0 | GC0 | GC0 |
| RGB for 256, 4k and 65k Color Mode | See Section 6.14 | See Section 6.14 | No Change |
| Partial: Start Address (PSL) | 0000h | 0000h | 0000h |
| Partial: End Address (PEL) | 013Fh | 013Fh | 013Fh |
| Scroll: Vertical scrolling | Off | Off | Off |
| Scroll: Top Fixed Area (TFA) | 0000h | 0000h | 0000h |
| Scroll: Scroll Area (VSA) | 0140h | 0140h | 0140h |
| Scroll: Bottom Fixed Area (BFA) | 0000h | 0000h | 0000h |
| Scroll Start Address (SSA) | 0000h | 0000h | 0000h |
| Tearing: On/Off | Off | Off | Off |
| Tearing Effect Mode *3) | 0 (Mode1) | 0 (Mode1) | 0 (Mode1) |
| Memory Data Access Control (MY/MX/MV/ML/RGB) | 0/0/0/0/0 | 0/0/0/0/0 | No Change |
| Interface Pixel Color Format | 6 (18-Bit/Pixel) | 6 (18-Bit/Pixel) | No Change |
| RDDPM | 08h | 08h | 08h |
| RDDMADCTR | 00h | 00h | No Change |
| RDDCOLMOD | 6 (18-Bit/Pixel) | 6 (18-Bit/Pixel) | No Change |
| RDDIM | 00h | 00h | 00h |
| RDDSM | 00h | 00h | 00h |
| RDDSDR | 00h | 00h | 00h |
| ID1 | 38h | 38h | 38h |
| ID2 | NV Value | NV Value | NV Value |
| ID3 | NV Value | NV Value | NV Value |
| RDDISBV | 00h | 00h | 00h |
| RDCTRLD | 00h | 00h | 00h |
| RDCABC | 00h | 00h | 00h |
| RDCABCMB | 00h | 00h | 00h |
| RDABCSDR | 00h | 00h | 00h |

*Notes 1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied.*

*Notes:2. Powered-On Reset finishes within 10µs after both VDD & VDDIO are applied.*

*Notes:3. TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.*

### 7.11.2. Module Input/Output Pins

#### 7.11.2.1. Output or Bi-directional (I/O) Pins

| Output or Bi-directional pins | After Power On | After Hardware Reset | After Software Reset |
|---|---|---|---|
| TE | Low | Low | Low |
| D7 to D0 (Output driver) | High-Z (Inactive) | High-Z (Inactive) | High-Z (Inactive) |
| BC | Low | Low | Low |

*Note: There will be no output from D7-D0 during Power On/Off sequence, Hardware Reset and Software Reset.*

#### 7.11.2.2. Input Pins

| Input pins | During Power On Process | After Power On | After Hardware Reset | After Software Reset | During Power Off Process |
|---|---|---|---|---|---|
| RESX | See 7.8 | Input valid | Input valid | Input valid | See 7.8 |
| CSX | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| D/CX | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| WRX | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| RDX | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| D7 to D0 | Input invalid | Input valid | Input valid | Input valid | Input invalid |
| P/SX | Input invalid | Input valid | Input valid | Input valid | Input invalid |

### 7.11.3. Reset Timing

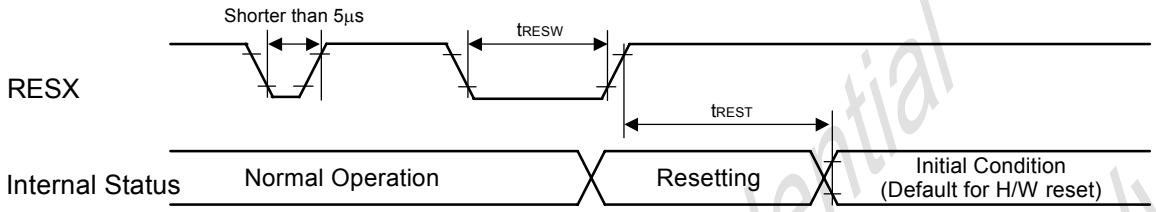



Table 7.11.3.1 Reset input timing

VSS=0V, VDDIO=1.6V to 3.6V, VDD=2.5V to 3.6V,Ta = -30 to 70°C)

| Symbol | Parameter | Related Pins | MIN | TYP | MAX | Note | Unit |
|---|---|---|---|---|---|---|---|
| $t_{RESW}$ | *1) Reset low pulse width | RESX | 10 | - | - | - | µs |
| $t_{REST}$ | *2) Reset complete time | - | - | - | 5 | When reset applied during Sleep in mode | ms |
| | | - | | - | 120 | When reset applied during Sleep out mode | ms |

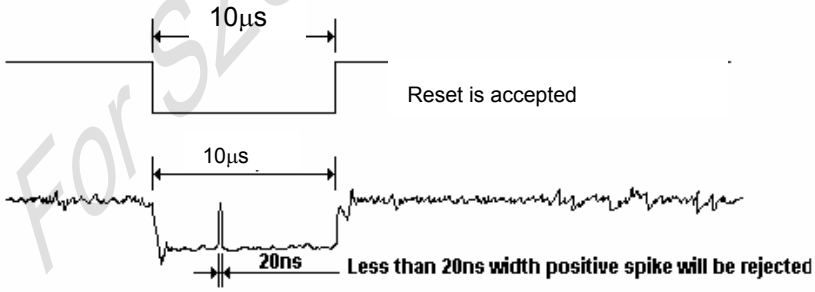
*Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.*

| RESX Pulse | Action |
|---|---|
| Shorter than 5µs | Reset Rejected |
| Longer than 10µs | Reset |
| Between 5µs and 10µs | Reset starts<br>(It depends on voltage and temperature condition.) |

*Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.*

*Note 3. During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.*

*Note 4. Spike Rejection also applies during a valid reset pulse as shown below:*




*Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.*

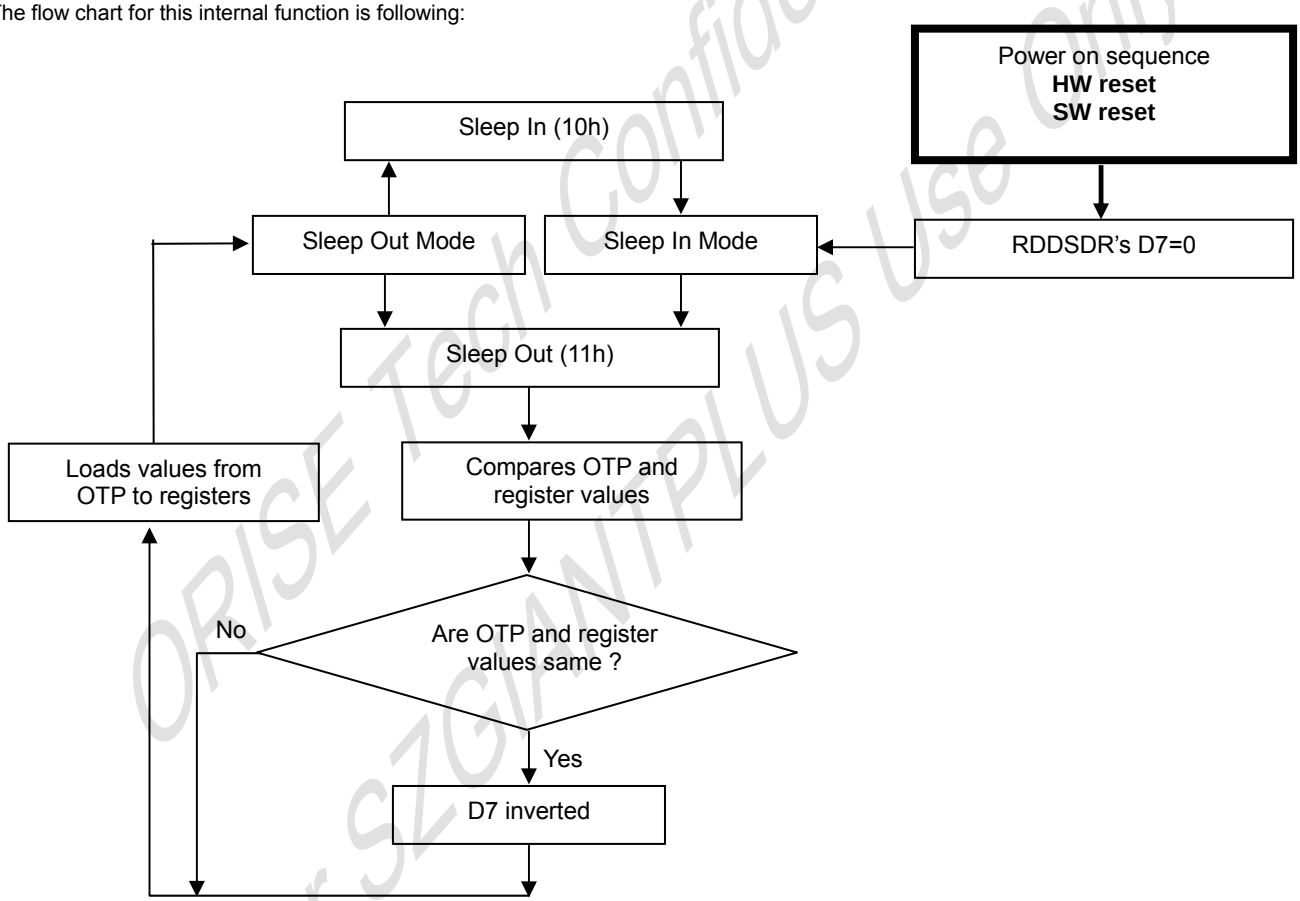
### 7.12. Sleep Out-Command and Self-Diagnostic Functions of the Display Module

#### 7.12.1. Register Loading Detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (one-time programming memory) to registers of the display controller is working properly.

There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit in “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= increased by 1).

The flow chart for this internal function is following:



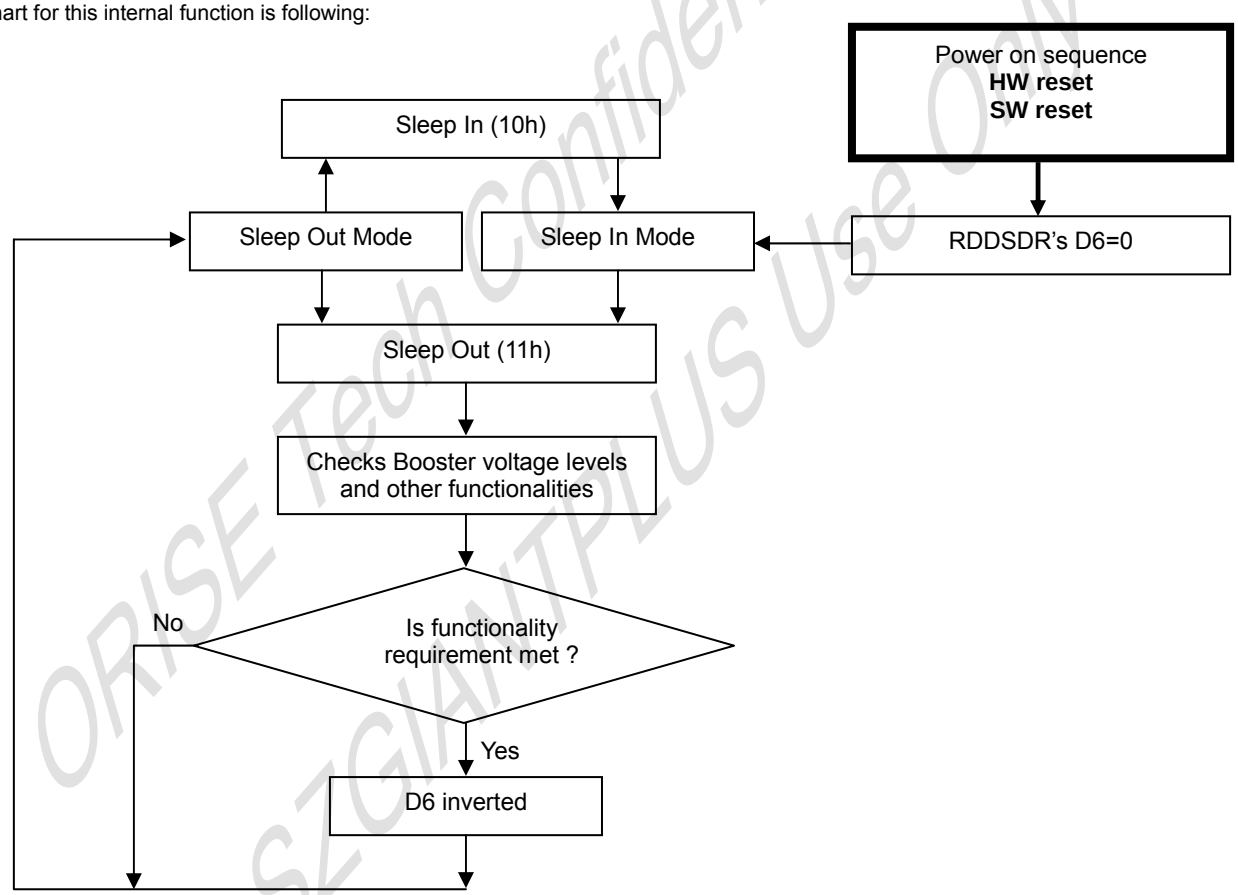

*Note: There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DDh), by the display module.*

### 7.12.2. Functionality Detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (only Booster voltage level). If functionality requirement is met, there is inverted (= increased by 1) a bit in “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1).

The flow chart for this internal function is following:




*Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.*

### 7.13. Oscillator

The chip has on-chip oscillator that does not require external components. This oscillator output signal is used for system clock generation for internal display operation.

### 7.14. System Colck Generator

The timing generator produces the various signals to dirver the internal circuitty. Internal chip operation is not affected by operations on the data bus.

### 7.15. Instruction Decoder and Register

The instruction decoder indentifies command words arriving at the interface and routes the following data bytes to their destination. The command set can be found in " Command" section.

### 7.16. Source Driver

The source driver block includes 240x3 source outputs (S1 to S720), which should be connected directly to the TFT-LCD. The source output signals are generated in the data processing block after the data is read out of the RAM and latched, which represent the simulatance selected rows.

### 7.17. Gate Driver

The gate dirver block include 320 chanel gate output (G1 to G320) which should be connected directly to the TFT-LCD.

#### 7.17.1. Gate Driver

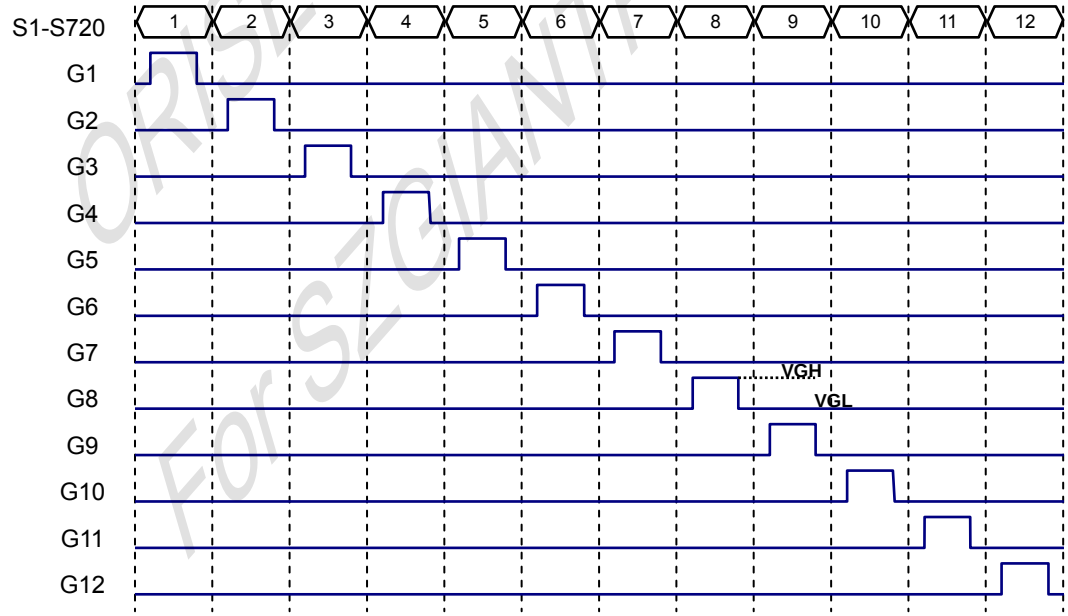



Fig. 7.20.1 Gate Driver Output Option 1

### 7.18. $\gamma$-CORRECTION FUNCTION

The OTM3206A adopts true 6-bit OP-AMP with adjustable $\gamma$-correction function to display in 262,144 colors. The adjustable $\gamma$-correction can be set by 14 groups of registers to determine eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers. Each register group can be set independently to other register groups.

### 7.19. $\gamma$-CORRECTION FUNCTION

## 8. ELECTRICAL SPECIFICATIONS

### 8.1. Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit | Note |
|---|---|---|---|---|
| Power Supply Voltage1 | VDD,VDDIO | -0.3~+4.6 | V | |
| Power Supply Voltage 2 | VCI1-VSS | -0.3~+4.6 | V | |
| Power Supply Voltage 3 | AVDD-VSS | -0.3~+6.5 | V | |
| Power Supply Voltage 4 | VSS-VCL | -0.3~+4.6 | V | |
| Power Supply Voltage 5 | VSS-VGL | -0.3~+14 | V | |
| Power Supply Voltage 6 | VGH-VGL | -0.3~+30 | V | |
| Input Voltage | Vt | -0.3~VDDIO+0.3 | V | |
| Operating Temperature | Topr | -30~+70 | ℃ | |
| Storage Temperature | Tstg | -40~+85 | ℃ | |

Note：1. The maximum applicable voltage on any pin with respect to 0V.

2. Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

### 8.2. DC Characteristic

(VDD=2.5V~3.6V, VDDIO = 1.6V~3.6V, Ta = -40℃ ~ 85℃)

| Parameter | Symbol | Conditions | Specification | | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | |
| **Power & Operation Voltage** | | | | | | | |
| Analog Operating voltage | VDD | Operating Voltage | 2.5 | 2.78 | 3.6 | V | |
| Logic Operating voltage | VDDIO | I/O supply voltage- | 1.6 | 1.8/2.78 | 3.6 | V | |
| Digital Operating voltage | VCC | Digital supply voltage | 1.6 | | 1.8 | V | |
| Gate Driver High voltage | VGH | | 9.0 | | 16.5 | V | |
| Gate Driver Low voltage | VGL | | -13.5 | | -6.5 | V | |
| Driver Supply voltage | | \|VGH-VGL\| | 19 | | 30 | V | |
| **Input / Output** | | | | | | | |
| Logic High level input voltage | VIH | | 0.7VDDIO | - | VDDIO | V | |
| Logic Low level input voltage | VIL | - | VSS | - | 0.3VDDIO | V | |
| Logic High level output voltage | VOH | IOH = -1.0mA | 0.8VDDIO | - | VDDIO | V | |
| Logic Low level output voltage | VOL | IOL = +1.0mA | VSS | - | 0.2VDDIO | V | |
| Logic High level input current | IIH | | | | 1 | μA | |
| Logic Low level input current | IIL | | -1 | | | μA | |
| Logic Input leakage current | IIL | VIN = VDDIO or VSS | -0.1 | - | +0.1 | μA | |
| **VCOM Operation** | | | | | | | |
| VCOM High voltage | VCOMH | Ccom=12nF | 2.5 | | 5.0 | V | |
| VCOM Low voltage | VCOML | Ccom=12nF | -2.5 | | 0.0 | V | |
| VCOM Amplitude voltage | VCOMA | \|VCOMH-VCOML\| | 4.0 | | 6.0 | V | |
| **Source Driver** | | | | | | | |
| Source output range | VSout | | 0.1 | | AVDD-0.1 | V | |
| Gamma reference voltage | GVDD | | 3.0 | | 5.0 | V | |
| Source output settling time | Tr | Below with 99% precision | | 15 | 20 | μs | |
| Output deviation voltage (Source output channel) | V,dev | Sout >=4.2V, Sout<=0.8V | | | 50 | mV | |
| | | 4.2V>Sout>0.8V | | | 30 | mV | |
| Output offset voltage | $V_{OFSET}$ | | | | 50 | mv | |
| **Booster Operation** | | | | | | | |
| Internal reference voltage | $V_{REF}$ | | | | 1 | % | |
| 1st Booster (VDDx2) voltage | AVDD | | 4.95 | | 6.0 | V | |
| 1st Booster (VDDx2) Drop voltage | VDDx2, drop | $I_{AVDD}$ = 1mA (include Panel loading) | | | 5% | % | |
| Linear range | $V_{Linear}$ | | 0.2 | | AVDD-0.2 | V | |

### 8.3. AC timing Characteristics

#### 8.3.1. Parallel Interface Characteristics 18, 16 ,9 or 8-bits bus (8080-series MCU)

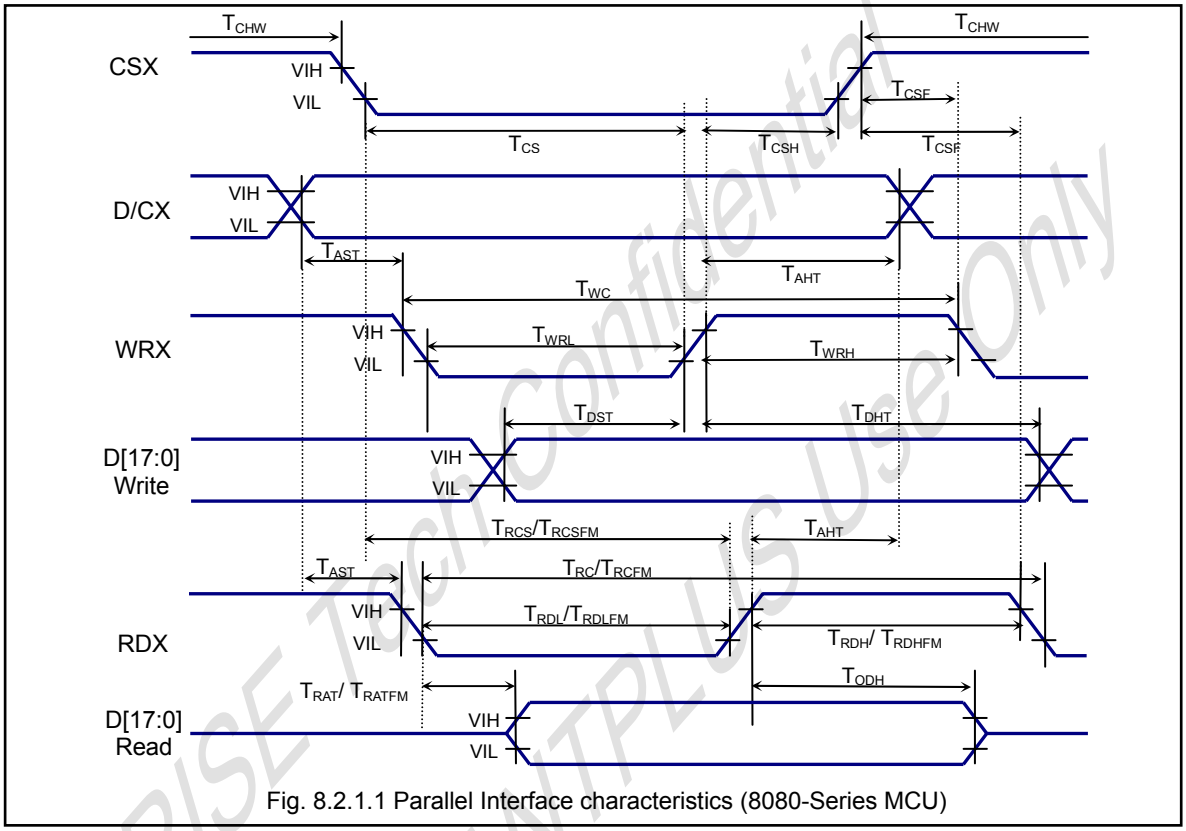



Fig. 8.2.1.1 Parallel Interface characteristics (8080-Series MCU)

Table 8.2.1.1: AC Characteristics for Parallel Interface18, 16, 9, 8-bits bus (8080-series MCU)

| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|---|---|---|---|---|---|---|
| D/CX | $T_{AST}$ | Address setup time | 0 | | ns | - |
| | $T_{AHT}$ | Address hold time (Write/Read) | 10 | | ns | |
| CSX | $T_{CHW}$ | Chip select “H” pulse width | 0 | | ns | -(3-transfer for one pixel) |
| | $T_{CS}$ | Chip select setup time (Write) | 15 | | ns | |
| | $T_{RCS}$ | Chip select setup time (Read ID) | 45 | | ns | |
| | $T_{RCSFM}$ | Chip select setup time (Read FM) | 355 | | ns | |
| | $T_{CSF}$ | Chip select wait time (Write/Read) | 10 | | ns | |
| | $T_{CSH}$ | Chip select hold time | 10 | | ns | |
| WRX | $T_{WC}$ | Write cycle | 66 | | ns | |
| | $T_{WRH}$ | Control pulse “H” duration | 15 | | ns | |
| | $T_{WRL}$ | Control pulse “L” duration | 15 | | ns | |
| RDX (ID) | $T_{RC}$ | Read cycle (ID) | 160 | | ns | When read ID data |
| | $T_{RDH}$ | Control pulse “H” duration (ID) | 90 | | ns | |
| | $T_{RDL}$ | Control pulse “L” duration (ID) | 45 | | ns | |
| RDX (FM) | $T_{RCFM}$ | Read cycle (FM) | 450 | | ns | When read from frame memory |
| | $T_{RDHFM}$ | Control pulse “H” duration (FM) | 90 | | ns | |
| | $T_{RDLFM}$ | Control pulse “L” duration (FM) | 355 | | ns | |
| D[17:0] | $T_{DST}$ | Data setup time | 10 | | ns | For maximum $C_L$=30pF<br>For minimum $C_L$=8pF |
| | $T_{DHT}$ | Data hold time | 10 | | ns | |
| | $T_{RAT}$ | Read access time (ID) | | 40 | ns | |
| | $T_{RATFM}$ | Read access time (FM) | | 340 | ns | |
| | $T_{ODH}$ | Output disable time | 20 | 80 | ns | |

Note 1: VDDIO=1.6 to 3.6V, VDD=2.5 to 3.6V, VSSA=VSS=0V, Ta=-30 to 70℃ (to +85℃ no damage)

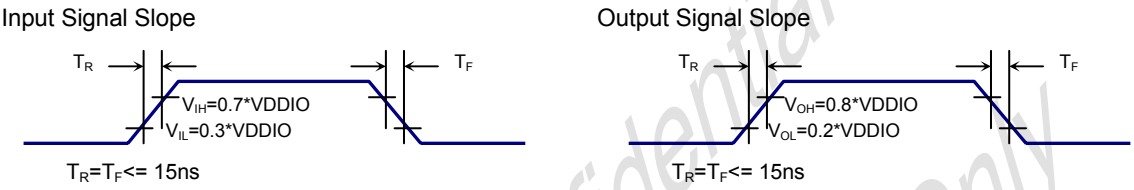



Fig. 8.2.1.2 Rising and Falling timing for Input and Output signal

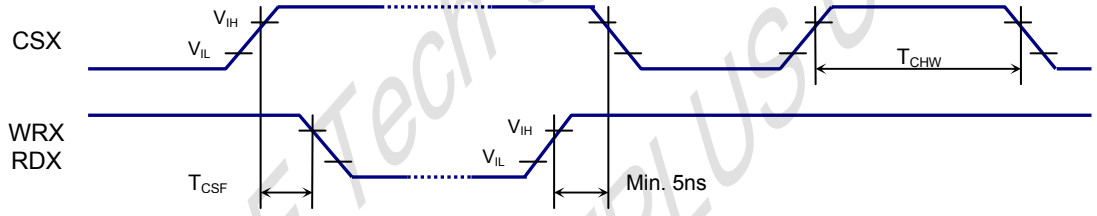



Fig.8.2.1.3 Chip selection (CSX) timing

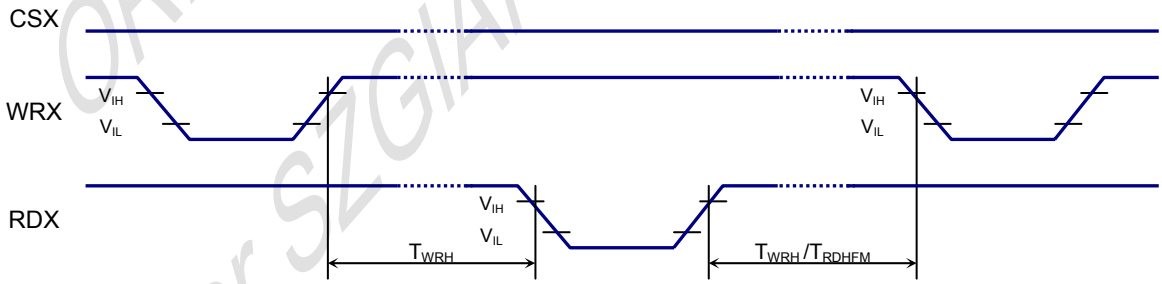



Fig. 8.2.1.4 Write to read and Read to write timing

NOTE: The input signal rise time and fall time (Tr, Tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDDIO for Input signals.

### 8.4. Parallel Interface Characteristics 18, 16 ,9 or 8-bits bus (6800-series MCU)

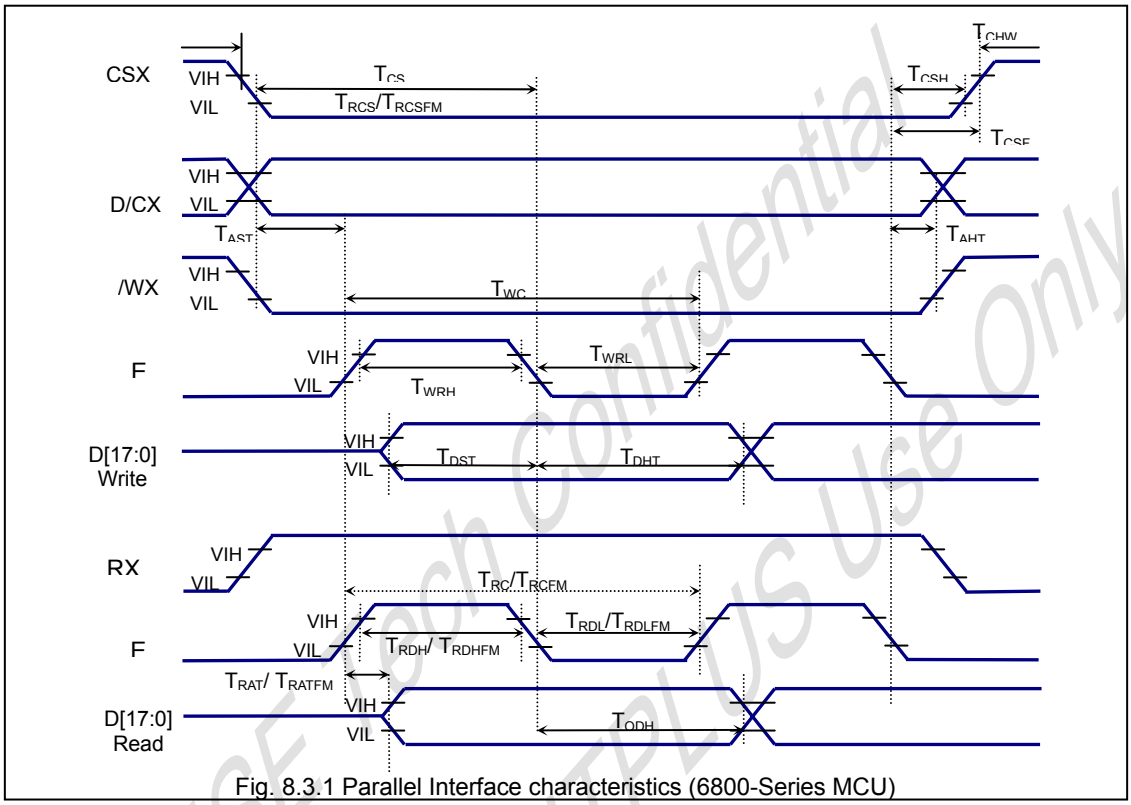



Fig. 8.3.1 Parallel Interface characteristics (6800-Series MCU)

Table 8.3.1: AC Characteristics for Parallel Interface 18, 16, 9, 8-bits bus (6800-series MCU)

| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|---|---|---|---|---|---|---|
| D/CX | $T_{AST}$ | Address setup time | 0 | | ns | - |
| | $T_{AHT}$ | Address hold time (Write/Read) | 10 | | ns | |
| CSX | $T_{CHW}$ | Chip select “H” pulse width | 0 | | ns | - |
| | $T_{CS}$ | Chip select setup time (Write) | 15 | | ns | |
| | $T_{RCS}$ | Chip select setup time (Read ID) | 45 | | ns | |
| | $T_{RCSFM}$ | Chip select setup time (Read FM) | 355 | | ns | |
| | $T_{CSF}$ | Chip select wait time (Write/Read) | 10 | | ns | |
| | $T_{CSH}$ | Chip select hold time | 10 | | ns | |
| WRX | $T_{WC}$ | Write cycle | 66 | | ns | |
| | $T_{WRH}$ | Control pulse “H” duration | 15 | | ns | |
| | $T_{WRL}$ | Control pulse “L” duration | 15 | | ns | |
| RDX (ID) | $T_{RC}$ | Read cycle (ID) | 160 | | ns | When read ID data |
| | $T_{RDH}$ | Control pulse “H” duration (ID) | 90 | | ns | |
| | $T_{RDL}$ | Control pulse “L” duration (ID) | 45 | | ns | |
| RDX (FM) | $T_{RCFM}$ | Read cycle (FM) | 450 | | ns | When read from frame memory |
| | $T_{RDHFM}$ | Control pulse “H” duration (FM) | 90 | | ns | |
| | $T_{RDLFM}$ | Control pulse “L” duration (FM) | 355 | | ns | |
| D[17:0] | $T_{DST}$ | Data setup time | 10 | | ns | For maximum $C_L$=30pF For minimum $C_L$=8pF |
| | $T_{DHT}$ | Data hold time | 10 | | ns | |
| | $T_{RAT}$ | Read access time (ID) | | 40 | ns | |
| | $T_{RATFM}$ | Read access time (FM) | | 340 | ns | |
| | $T_{ODH}$ | Output disable time | 20 | 80 | ns | |

Note 1: VDDIO=1.6 to 3.6V, VDD=2.5 to 3.6V, VSSA=VSS=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDDIO for Input signals.

### 8.5. Serial Interface Characteristics (3-pin Serial)

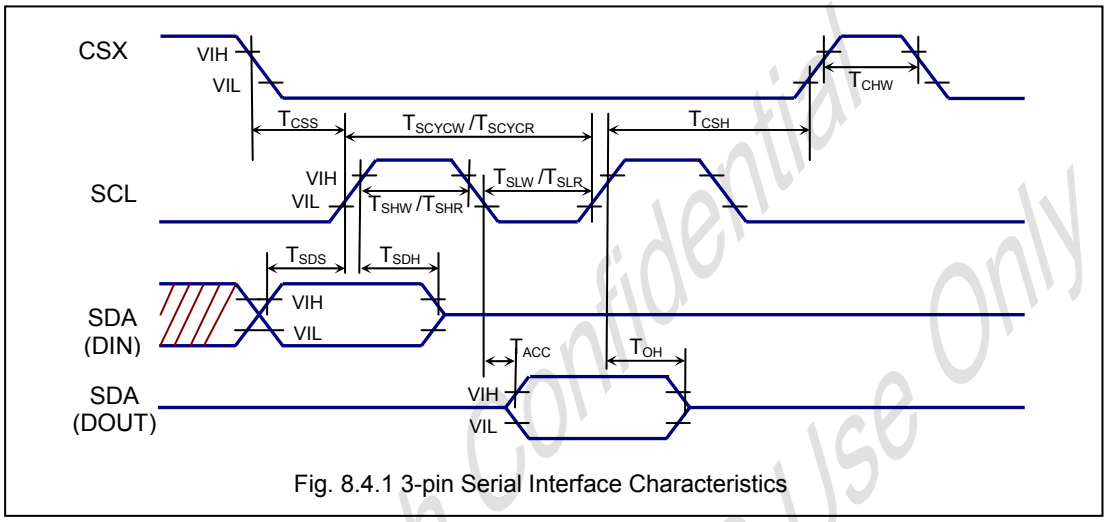



Fig. 8.4.1 3-pin Serial Interface Characteristics

Table 8.4.1: 3-pin Serial Interface Characteristics

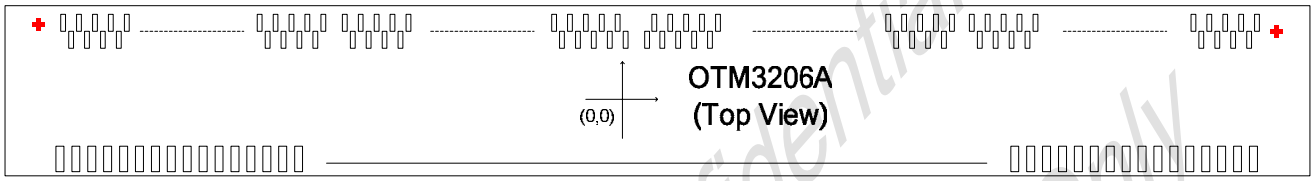
| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|---|---|---|---|---|---|---|
| CSX | $T_{CSS}$ | Chip select setup time | 15 | | ns | |
| | $T_{CSH}$ | Chip select hold time | 15 | | ns | |
| | $T_{CHW}$ | Chip select setup time | 40 | | ns | |
| SCL | $T_{SCYCW}$ | Serial clock cycle (Write) | 66 | | ns | - |
| | $T_{SHW}$ | SCL “H” pulse width (Write) | 10 | | ns | |
| | $T_{SLW}$ | SCL “L” pulse width (Write) | 10 | | ns | |
| | $T_{SCYCR}$ | Serial clock cycle (Read) | 150 | | ns | |
| | $T_{SHR}$ | SCL “H” pulse width (Read) | 60 | | ns | |
| | $T_{SLR}$ | SCL “L” pulse width (Read) | 60 | | ns | |
| SDA (DIN) (DOUT) | $T_{SDS}$ | Data setup time | 10 | | ns | |
| | $T_{SDH}$ | Data hold time | 10 | | ns | |
| | $T_{ACC}$ | Access time | 10 | | ns | For maximum $C_L$=30pF |
| | $T_{OH}$ | Output disable time | 15 | 50 | ns | For minimum $C_L$=8pF |

Note 1: VDDIO=1.6 to 3.6V, VDD=2.5 to 3.6V, VSSA=VSS=0V, Ta=-30 to 70℃ (to +85℃ no damage)

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDDIO for Input signals.

## 9. CHIP INFORMATION

### 9.1. PAD Assignment

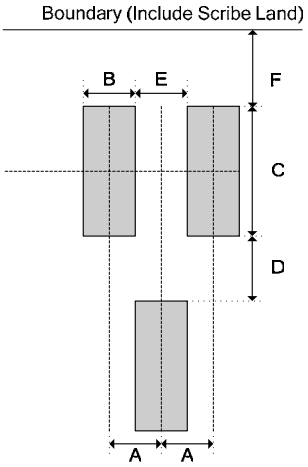



### 9.2. PAD Dimension

| Item | PAD No. | Size | | Unit |
|---|---|---|---|---|
| | | X | Y | |
| Chip Size | - | 15580 | 750 | μm |
| Chip thickness | - | 300 ± 20 | | |
| Pad pitch | 1~185 | 80 | - | |
| | 186~1235 | 14 | - | |
| Pad Size | 1~185 | 62 | 90 | |
| | 186~1235 | 14 | 85 | |

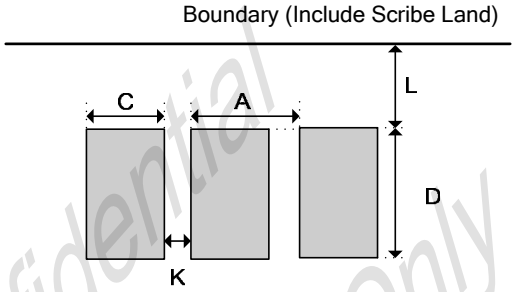
**Note1:** Chip size included scribe line.

### 9.2.1. Output Pads




| Item | Sumbol | Size |
|---|---|---|
| Bump Pitch | A | 14 um |
| Bump Width | B | 13.5 um |
| Bump height | C | 85 um |
| Bump space 1 | D | 20 um |
| Bump space 2 | E | 14.5 um |
| Bump area | BxC | 1147.5 $um^2$ |
| Chip boundary | F | 96.5 um |

### 9.2.2. Input Pads




| Item | Sumbol | Size |
|---|---|---|
| Bump Pitch1 | A | 80 um |
| Bump Width1 | C | 62 um |
| Bump Height | D | 90 um |
| Bump space | K | 18 um |
| Bump area1 | CxD | 5580 $um^2$ |
| Chip boundary | L | 99 um |

### 9.3. Bump Characteristics

| Item | Standard | Note |
|---|---|---|
| Bump Hardness | 90Hv | ± 20Hv |
| Bump Height | 15μm | ± 3μm |
| Co-planarity (in Chip) | R≦ 2μm | R : Max-Min |
| Roughness (in Bump) | R≦ 2μm | R : Max-Min |
| Bump Size | Long side ± 2.5μm, short side ± 2μm | X/Y: bump size |
| Shear Force | >5g/mil^2 | |

### 9.4. PAD Locations

| PAD No. | PAD Name | X | Y |
|---|---|---|---|
| 1 | DUMMY1 | -7360 | -231 |
| 2 | VCOM | -7280 | -231 |
| 3 | VCOM | -7200 | -231 |
| 4 | VCOM | -7120 | -231 |
| 5 | VCOM | -7040 | -231 |
| 6 | VCOM | -6960 | -231 |
| 7 | TEST1 | -6880 | -231 |
| 8 | BC | -6800 | -231 |
| 9 | BC | -6720 | -231 |
| 10 | VSSA | -6640 | -231 |
| 11 | VSSA | -6560 | -231 |
| 12 | VCOML | -6480 | -231 |
| 13 | VCOMH | -6400 | -231 |
| 14 | GVDD | -6320 | -231 |
| 15 | VSSA | -6240 | -231 |
| 16 | VSSA | -6160 | -231 |
| 17 | VSSA | -6080 | -231 |
| 18 | VSSA | -6000 | -231 |
| 19 | VSSA | -5920 | -231 |
| 20 | VSSA | -5840 | -231 |
| 21 | VSSA | -5760 | -231 |
| 22 | C3M | -5680 | -231 |
| 23 | C3M | -5600 | -231 |
| 24 | C3M | -5520 | -231 |
| 25 | C3P | -5440 | -231 |
| 26 | C3P | -5360 | -231 |
| 27 | C3P | -5280 | -231 |
| 28 | C4M | -5200 | -231 |
| 29 | C4M | -5120 | -231 |
| 30 | C4M | -5040 | -231 |
| 31 | C4P | -4960 | -231 |
| 32 | C4P | -4880 | -231 |
| 33 | C4P | -4800 | -231 |
| 34 | VGH | -4720 | -231 |
| 35 | VGH | -4640 | -231 |
| 36 | VGH | -4560 | -231 |
| 37 | VGH | -4480 | -231 |
| 38 | VGL | -4400 | -231 |
| 39 | VGL | -4320 | -231 |
| 40 | VGL | -4240 | -231 |
| 41 | VGL | -4160 | -231 |
| 42 | VGL | -4080 | -231 |
| 43 | C5P | -4000 | -231 |
| 44 | C5P | -3920 | -231 |
| 45 | C5P | -3840 | -231 |
| 46 | C5P | -3760 | -231 |
| 47 | C5P | -3680 | -231 |
| 48 | C5M | -3600 | -231 |
| 49 | C5M | -3520 | -231 |
| 50 | C5M | -3440 | -231 |
| 51 | C5M | -3360 | -231 |
| 52 | C5M | -3280 | -231 |
| 53 | VSS | -3200 | -231 |
| 54 | VSS | -3120 | -231 |
| 55 | VSS | -3040 | -231 |
| 56 | VSS | -2960 | -231 |
| 57 | VSS | -2880 | -231 |
| 58 | VSS | -2800 | -231 |
| 59 | VSS | -2720 | -231 |
| 60 | C2M | -2640 | -231 |
| 61 | C2M | -2560 | -231 |
| 62 | C2M | -2480 | -231 |
| 63 | C2M | -2400 | -231 |
| 64 | C2M | -2320 | -231 |
| 65 | C2M | -2240 | -231 |
| 66 | C2P | -2160 | -231 |
| 67 | C2P | -2080 | -231 |
| 68 | C2P | -2000 | -231 |
| 69 | C2P | -1920 | -231 |
| 70 | C2P | -1840 | -231 |
| 71 | C2P | -1760 | -231 |
| 72 | VCL | -1680 | -231 |
| 73 | VCL | -1600 | -231 |
| 74 | VCL | -1520 | -231 |
| 75 | VCL | -1440 | -231 |
| 76 | VCL | -1360 | -231 |
| 77 | VCL | -1280 | -231 |
| 78 | C1M | -1200 | -231 |
| 79 | C1M | -1120 | -231 |
| 80 | C1M | -1040 | -231 |
| 81 | C1M | -960 | -231 |
| 82 | C1M | -880 | -231 |
| 83 | C1M | -800 | -231 |
| 84 | C1P | -720 | -231 |
| 85 | C1P | -640 | -231 |
| 86 | C1P | -560 | -231 |
| 87 | C1P | -480 | -231 |
| 88 | C1P | -400 | -231 |
| 89 | C1P | -320 | -231 |
| 90 | VDDA | -240 | -231 |
| 91 | VDDA | -160 | -231 |
| 92 | VDDA | -80 | -231 |
| 93 | VDDA | 0 | -231 |
| 94 | VDDA | 80 | -231 |
| 95 | VDDA | 160 | -231 |
| 96 | VCI1 | 240 | -231 |
| 97 | TEST2 | 320 | -231 |
| 98 | CSX | 400 | -231 |
| 99 | RDX | 480 | -231 |
| 100 | TE | 560 | -231 |
| 101 | WRX | 640 | -231 |
| 102 | DCX | 720 | -231 |
| 103 | VDD_OTP | 800 | -231 |
| 104 | VDD_OTP | 880 | -231 |
| 105 | VDD_OTP | 960 | -231 |
| 106 | VDDIO | 1040 | -231 |
| 107 | VDDIO | 1120 | -231 |
| 108 | VDDIO | 1200 | -231 |
| 109 | VDDIO | 1280 | -231 |
| 110 | VDDIO | 1360 | -231 |
| 111 | VDD_BC | 1440 | -231 |
| 112 | VDD | 1520 | -231 |
| 113 | VDD | 1600 | -231 |
| 114 | VDD | 1680 | -231 |
| 115 | VDD | 1760 | -231 |
| 116 | VDD | 1840 | -231 |
| 117 | VDD | 1920 | -231 |
| 118 | VDD | 2000 | -231 |
| 119 | VDD | 2080 | -231 |
| 120 | VDD | 2160 | -231 |
| 121 | VDD | 2240 | -231 |
| 122 | VDD | 2320 | -231 |
| 123 | VSS | 2400 | -231 |
| 124 | RESX | 2480 | -231 |
| 125 | RESX | 2560 | -231 |
| 126 | EXTC | 2640 | -231 |
| 127 | D7 | 2720 | -231 |
| 128 | D6 | 2800 | -231 |
| 129 | D5 | 2880 | -231 |
| 130 | D4 | 2960 | -231 |
| 131 | VSS | 3040 | -231 |
| 132 | D3 | 3120 | -231 |
| 133 | D2 | 3200 | -231 |
| 134 | D1 | 3280 | -231 |
| 135 | D0 | 3360 | -231 |
| 136 | VSS | 3440 | -231 |
| 137 | SDA | 3520 | -231 |
| 138 | SDA | 3600 | -231 |
| 139 | D17 | 3680 | -231 |
| 140 | D16 | 3760 | -231 |
| 141 | D15 | 3840 | -231 |
| 142 | D14 | 3920 | -231 |
| 143 | D13 | 4000 | -231 |
| 144 | D12 | 4080 | -231 |
| 145 | D11 | 4160 | -231 |
| 146 | D10 | 4240 | -231 |
| 147 | D9 | 4320 | -231 |
| 148 | D8 | 4400 | -231 |
| 149 | TEST3 | 4480 | -231 |
| 150 | TEST4 | 4560 | -231 |
| 151 | TEST5 | 4640 | -231 |
| 152 | TEST6 | 4720 | -231 |
| 153 | TEST7 | 4800 | -231 |
| 154 | TEST8 | 4880 | -231 |
| 155 | TEST9 | 4960 | -231 |
| 156 | TEST10 | 5040 | -231 |

| PAD No. | PAD Name | X | Y |
|---|---|---|---|
| 157 | VSS | 5120 | -231 |
| 158 | IM3 | 5200 | -231 |
| 159 | IM2 | 5280 | -231 |
| 160 | IM1 | 5360 | -231 |
| 161 | IM0 | 5440 | -231 |
| 162 | VDDIO | 5520 | -231 |
| 163 | VREF | 5600 | -231 |
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| 165 | VDD_18V | 5760 | -231 |
| 166 | VDD_18V | 5840 | -231 |
| 167 | VDD_18V | 5920 | -231 |
| 168 | VDD_18V | 6000 | -231 |
| 169 | VSS | 6080 | -231 |
| 170 | VSS | 6160 | -231 |
| 171 | VSS | 6240 | -231 |
| 172 | VSS | 6320 | -231 |
| 173 | VSS | 6400 | -231 |
| 174 | VSS | 6480 | -231 |
| 175 | VSS | 6560 | -231 |
| 176 | TEST11 | 6640 | -231 |
| 177 | TEST12 | 6720 | -231 |
| 178 | VSSA | 6800 | -231 |
| 179 | VSSA | 6880 | -231 |
| 180 | VCOM | 6960 | -231 |
| 181 | VCOM | 7040 | -231 |
| 182 | VCOM | 7120 | -231 |
| 183 | VCOM | 7200 | -231 |
| 184 | VCOM | 7280 | -231 |
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| 191 | G314 | 7333 | 131 |
| 192 | G312 | 7319 | 236 |
| 193 | G310 | 7305 | 131 |
| 194 | G308 | 7291 | 236 |
| 195 | G306 | 7277 | 131 |
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| 197 | G302 | 7249 | 131 |
| 198 | G300 | 7235 | 236 |
| 199 | G298 | 7221 | 131 |
| 200 | G296 | 7207 | 236 |
| 201 | G294 | 7193 | 131 |
| 202 | G292 | 7179 | 236 |
| 203 | G290 | 7165 | 131 |
| 204 | G288 | 7151 | 236 |
| 205 | G286 | 7137 | 131 |
| 206 | G284 | 7123 | 236 |
| 207 | G282 | 7109 | 131 |
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| 211 | G274 | 7053 | 131 |
| 212 | G272 | 7039 | 236 |
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| 214 | G268 | 7011 | 236 |
| 215 | G266 | 6997 | 131 |
| 216 | G264 | 6983 | 236 |
| 217 | G262 | 6969 | 131 |
| 218 | G260 | 6955 | 236 |
| 219 | G258 | 6941 | 131 |
| 220 | G256 | 6927 | 236 |
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| 222 | G252 | 6899 | 236 |
| 223 | G250 | 6885 | 131 |
| 224 | G248 | 6871 | 236 |
| 225 | G246 | 6857 | 131 |
| 226 | G244 | 6843 | 236 |
| 227 | G242 | 6829 | 131 |
| 228 | G240 | 6815 | 236 |
| 229 | G238 | 6801 | 131 |
| 230 | G236 | 6787 | 236 |
| 231 | G234 | 6773 | 131 |
| 232 | G232 | 6759 | 236 |
| 233 | G230 | 6745 | 131 |
| 234 | G228 | 6731 | 236 |
| 235 | G226 | 6717 | 131 |
| 236 | G224 | 6703 | 236 |
| 237 | G222 | 6689 | 131 |
| 238 | G220 | 6675 | 236 |
| 239 | G218 | 6661 | 131 |
| 240 | G216 | 6647 | 236 |
| 241 | G214 | 6633 | 131 |
| 242 | G212 | 6619 | 236 |
| 243 | G210 | 6605 | 131 |
| 244 | G208 | 6591 | 236 |
| 245 | G206 | 6577 | 131 |
| 246 | G204 | 6563 | 236 |
| 247 | G202 | 6549 | 131 |
| 248 | G200 | 6535 | 236 |
| 249 | G198 | 6521 | 131 |
| 250 | G196 | 6507 | 236 |
| 251 | G194 | 6493 | 131 |
| 252 | G192 | 6479 | 236 |
| 253 | G190 | 6465 | 131 |
| 254 | G188 | 6451 | 236 |
| 255 | G186 | 6437 | 131 |
| 256 | G184 | 6423 | 236 |
| 257 | G182 | 6409 | 131 |
| 258 | G180 | 6395 | 236 |
| 259 | G178 | 6381 | 131 |
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| 261 | G174 | 6353 | 131 |
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| 266 | G164 | 6283 | 236 |
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| 268 | G160 | 6255 | 236 |
| 269 | G158 | 6241 | 131 |
| 270 | G156 | 6227 | 236 |
| 271 | G154 | 6213 | 131 |
| 272 | G152 | 6199 | 236 |
| 273 | G150 | 6185 | 131 |
| 274 | G148 | 6171 | 236 |
| 275 | G146 | 6157 | 131 |
| 276 | G144 | 6143 | 236 |
| 277 | G142 | 6129 | 131 |
| 278 | G140 | 6115 | 236 |
| 279 | G138 | 6101 | 131 |
| 280 | G136 | 6087 | 236 |
| 281 | G134 | 6073 | 131 |
| 282 | G132 | 6059 | 236 |
| 283 | G130 | 6045 | 131 |
| 284 | G128 | 6031 | 236 |
| 285 | G126 | 6017 | 131 |
| 286 | G124 | 6003 | 236 |
| 287 | G122 | 5989 | 131 |
| 288 | G120 | 5975 | 236 |
| 289 | G118 | 5961 | 131 |
| 290 | G116 | 5947 | 236 |
| 291 | G114 | 5933 | 131 |
| 292 | G112 | 5919 | 236 |
| 293 | G110 | 5905 | 131 |
| 294 | G108 | 5891 | 236 |
| 295 | G106 | 5877 | 131 |
| 296 | G104 | 5863 | 236 |
| 297 | G102 | 5849 | 131 |
| 298 | G100 | 5835 | 236 |
| 299 | G98 | 5821 | 131 |
| 300 | G96 | 5807 | 236 |
| 301 | G94 | 5793 | 131 |
| 302 | G92 | 5779 | 236 |
| 303 | G90 | 5765 | 131 |
| 304 | G88 | 5751 | 236 |
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| 306 | G84 | 5723 | 236 |
| 307 | G82 | 5709 | 131 |
| 308 | G80 | 5695 | 236 |
| 309 | G78 | 5681 | 131 |
| 310 | G76 | 5667 | 236 |
| 311 | G74 | 5653 | 131 |
| 312 | G72 | 5639 | 236 |
| 313 | G70 | 5625 | 131 |
| 314 | G68 | 5611 | 236 |
| 315 | G66 | 5597 | 131 |

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| 317 | G62 | 5569 | 131 |
| 318 | G60 | 5555 | 236 |
| 319 | G58 | 5541 | 131 |
| 320 | G56 | 5527 | 236 |
| 321 | G54 | 5513 | 131 |
| 322 | G52 | 5499 | 236 |
| 323 | G50 | 5485 | 131 |
| 324 | G48 | 5471 | 236 |
| 325 | G46 | 5457 | 131 |
| 326 | G44 | 5443 | 236 |
| 327 | G42 | 5429 | 131 |
| 328 | G40 | 5415 | 236 |
| 329 | G38 | 5401 | 131 |
| 330 | G36 | 5387 | 236 |
| 331 | G34 | 5373 | 131 |
| 332 | G32 | 5359 | 236 |
| 333 | G30 | 5345 | 131 |
| 334 | G28 | 5331 | 236 |
| 335 | G26 | 5317 | 131 |
| 336 | G24 | 5303 | 236 |
| 337 | G22 | 5289 | 131 |
| 338 | G20 | 5275 | 236 |
| 339 | G18 | 5261 | 131 |
| 340 | G16 | 5247 | 236 |
| 341 | G14 | 5233 | 131 |
| 342 | G12 | 5219 | 236 |
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| 353 | S717 | 5025 | 236 |
| 354 | S716 | 5011 | 131 |
| 355 | S715 | 4997 | 236 |
| 356 | S714 | 4983 | 131 |
| 357 | S713 | 4969 | 236 |
| 358 | S712 | 4955 | 131 |
| 359 | S711 | 4941 | 236 |
| 360 | S710 | 4927 | 131 |
| 361 | S709 | 4913 | 236 |
| 362 | S708 | 4899 | 131 |
| 363 | S707 | 4885 | 236 |
| 364 | S706 | 4871 | 131 |
| 365 | S705 | 4857 | 236 |
| 366 | S704 | 4843 | 131 |
| 367 | S703 | 4829 | 236 |
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| 371 | S699 | 4773 | 236 |
| 372 | S698 | 4759 | 131 |
| 373 | S697 | 4745 | 236 |
| 374 | S696 | 4731 | 131 |
| 375 | S695 | 4717 | 236 |
| 376 | S694 | 4703 | 131 |
| 377 | S693 | 4689 | 236 |
| 378 | S692 | 4675 | 131 |
| 379 | S691 | 4661 | 236 |
| 380 | S690 | 4647 | 131 |
| 381 | S689 | 4633 | 236 |
| 382 | S688 | 4619 | 131 |
| 383 | S687 | 4605 | 236 |
| 384 | S686 | 4591 | 131 |
| 385 | S685 | 4577 | 236 |
| 386 | S684 | 4563 | 131 |
| 387 | S683 | 4549 | 236 |
| 388 | S682 | 4535 | 131 |
| 389 | S681 | 4521 | 236 |
| 390 | S680 | 4507 | 131 |
| 391 | S679 | 4493 | 236 |
| 392 | S678 | 4479 | 131 |
| 393 | S677 | 4465 | 236 |
| 394 | S676 | 4451 | 131 |
| 395 | S675 | 4437 | 236 |
| 396 | S674 | 4423 | 131 |
| 397 | S673 | 4409 | 236 |
| 398 | S672 | 4395 | 131 |
| 399 | S671 | 4381 | 236 |
| 400 | S670 | 4367 | 131 |
| 401 | S669 | 4353 | 236 |
| 402 | S668 | 4339 | 131 |
| 403 | S667 | 4325 | 236 |
| 404 | S666 | 4311 | 131 |
| 405 | S665 | 4297 | 236 |
| 406 | S664 | 4283 | 131 |
| 407 | S663 | 4269 | 236 |
| 408 | S662 | 4255 | 131 |
| 409 | S661 | 4241 | 236 |
| 410 | S660 | 4227 | 131 |
| 411 | S659 | 4213 | 236 |
| 412 | S658 | 4199 | 131 |
| 413 | S657 | 4185 | 236 |
| 414 | S656 | 4171 | 131 |
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| 416 | S654 | 4143 | 131 |
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| 418 | S652 | 4115 | 131 |
| 419 | S651 | 4101 | 236 |
| 420 | S650 | 4087 | 131 |
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| 425 | S645 | 4017 | 236 |
| 426 | S644 | 4003 | 131 |
| 427 | S643 | 3989 | 236 |
| 428 | S642 | 3975 | 131 |
| 429 | S641 | 3961 | 236 |
| 430 | S640 | 3947 | 131 |
| 431 | S639 | 3933 | 236 |
| 432 | S638 | 3919 | 131 |
| 433 | S637 | 3905 | 236 |
| 434 | S636 | 3891 | 131 |
| 435 | S635 | 3877 | 236 |
| 436 | S634 | 3863 | 131 |
| 437 | S633 | 3849 | 236 |
| 438 | S632 | 3835 | 131 |
| 439 | S631 | 3821 | 236 |
| 440 | S630 | 3807 | 131 |
| 441 | S629 | 3793 | 236 |
| 442 | S628 | 3779 | 131 |
| 443 | S627 | 3765 | 236 |
| 444 | S626 | 3751 | 131 |
| 445 | S625 | 3737 | 236 |
| 446 | S624 | 3723 | 131 |
| 447 | S623 | 3709 | 236 |
| 448 | S622 | 3695 | 131 |
| 449 | S621 | 3681 | 236 |
| 450 | S620 | 3667 | 131 |
| 451 | S619 | 3653 | 236 |
| 452 | S618 | 3639 | 131 |
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| 454 | S616 | 3611 | 131 |
| 455 | S615 | 3597 | 236 |
| 456 | S614 | 3583 | 131 |
| 457 | S613 | 3569 | 236 |
| 458 | S612 | 3555 | 131 |
| 459 | S611 | 3541 | 236 |
| 460 | S610 | 3527 | 131 |
| 461 | S609 | 3513 | 236 |
| 462 | S608 | 3499 | 131 |
| 463 | S607 | 3485 | 236 |
| 464 | S606 | 3471 | 131 |
| 465 | S605 | 3457 | 236 |
| 466 | S604 | 3443 | 131 |
| 467 | S603 | 3429 | 236 |
| 468 | S602 | 3415 | 131 |
| 469 | S601 | 3401 | 236 |
| 470 | S600 | 3387 | 131 |
| 471 | S599 | 3373 | 236 |
| 472 | S598 | 3359 | 131 |
| 473 | S597 | 3345 | 236 |
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| 475 | S595 | 3317 | 236 |
| 476 | S594 | 3303 | 131 |
| 477 | S593 | 3289 | 236 |
| 478 | S592 | 3275 | 131 |
| 479 | S591 | 3261 | 236 |
| 480 | S590 | 3247 | 131 |
| 481 | S589 | 3233 | 236 |
| 482 | S588 | 3219 | 131 |
| 483 | S587 | 3205 | 236 |
| 484 | S586 | 3191 | 131 |
| 485 | S585 | 3177 | 236 |
| 486 | S584 | 3163 | 131 |
| 487 | S583 | 3149 | 236 |
| 488 | S582 | 3135 | 131 |
| 489 | S581 | 3121 | 236 |
| 490 | S580 | 3107 | 131 |
| 491 | S579 | 3093 | 236 |
| 492 | S578 | 3079 | 131 |
| 493 | S577 | 3065 | 236 |
| 494 | S576 | 3051 | 131 |
| 495 | S575 | 3037 | 236 |
| 496 | S574 | 3023 | 131 |
| 497 | S573 | 3009 | 236 |
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| 499 | S571 | 2981 | 236 |
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| 501 | S569 | 2953 | 236 |
| 502 | S568 | 2939 | 131 |
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| 504 | S566 | 2911 | 131 |
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| 507 | S563 | 2869 | 236 |
| 508 | S562 | 2855 | 131 |
| 509 | S561 | 2841 | 236 |
| 510 | S560 | 2827 | 131 |
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| 513 | S557 | 2785 | 236 |
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| 536 | S534 | 2463 | 131 |
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| 538 | S532 | 2435 | 131 |
| 539 | S531 | 2421 | 236 |
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| 545 | S525 | 2337 | 236 |
| 546 | S524 | 2323 | 131 |
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| 548 | S522 | 2295 | 131 |
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| 600 | S470 | 1567 | 131 |
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| 643 | S427 | 965 | 236 |
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| 649 | S421 | 881 | 236 |
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| 693 | S377 | 265 | 236 |
| 694 | S376 | 251 | 131 |
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| 696 | S374 | 223 | 131 |
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| 731 | S341 | -307 | 131 |
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| 733 | S339 | -335 | 131 |
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| 737 | S335 | -391 | 131 |
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| 746 | S326 | -517 | 236 |
| 747 | S325 | -531 | 131 |
| 748 | S324 | -545 | 236 |
| 749 | S323 | -559 | 131 |
| 750 | S322 | -573 | 236 |
| 751 | S321 | -587 | 131 |
| 752 | S320 | -601 | 236 |
| 753 | S319 | -615 | 131 |
| 754 | S318 | -629 | 236 |
| 755 | S317 | -643 | 131 |
| 756 | S316 | -657 | 236 |
| 757 | S315 | -671 | 131 |
| 758 | S314 | -685 | 236 |
| 759 | S313 | -699 | 131 |
| 760 | S312 | -713 | 236 |
| 761 | S311 | -727 | 131 |
| 762 | S310 | -741 | 236 |
| 763 | S309 | -755 | 131 |
| 764 | S308 | -769 | 236 |
| 765 | S307 | -783 | 131 |
| 766 | S306 | -797 | 236 |
| 767 | S305 | -811 | 131 |
| 768 | S304 | -825 | 236 |
| 769 | S303 | -839 | 131 |
| 770 | S302 | -853 | 236 |
| 771 | S301 | -867 | 131 |
| 772 | S300 | -881 | 236 |
| 773 | S299 | -895 | 131 |
| 774 | S298 | -909 | 236 |
| 775 | S297 | -923 | 131 |
| 776 | S296 | -937 | 236 |
| 777 | S295 | -951 | 131 |
| 778 | S294 | -965 | 236 |
| 779 | S293 | -979 | 131 |
| 780 | S292 | -993 | 236 |
| 781 | S291 | -1007 | 131 |
| 782 | S290 | -1021 | 236 |
| 783 | S289 | -1035 | 131 |
| 784 | S288 | -1049 | 236 |
| 785 | S287 | -1063 | 131 |
| 786 | S286 | -1077 | 236 |
| 787 | S285 | -1091 | 131 |
| 788 | S284 | -1105 | 236 |
| 789 | S283 | -1119 | 131 |
| 790 | S282 | -1133 | 236 |
| 791 | S281 | -1147 | 131 |
| 792 | S280 | -1161 | 236 |

| PAD No. | PAD Name | X | Y |
|---|---|---|---|
| 793 | S279 | -1175 | 131 |
| 794 | S278 | -1189 | 236 |
| 795 | S277 | -1203 | 131 |
| 796 | S276 | -1217 | 236 |
| 797 | S275 | -1231 | 131 |
| 798 | S274 | -1245 | 236 |
| 799 | S273 | -1259 | 131 |
| 800 | S272 | -1273 | 236 |
| 801 | S271 | -1287 | 131 |
| 802 | S270 | -1301 | 236 |
| 803 | S269 | -1315 | 131 |
| 804 | S268 | -1329 | 236 |
| 805 | S267 | -1343 | 131 |
| 806 | S266 | -1357 | 236 |
| 807 | S265 | -1371 | 131 |
| 808 | S264 | -1385 | 236 |
| 809 | S263 | -1399 | 131 |
| 810 | S262 | -1413 | 236 |
| 811 | S261 | -1427 | 131 |
| 812 | S260 | -1441 | 236 |
| 813 | S259 | -1455 | 131 |
| 814 | S258 | -1469 | 236 |
| 815 | S257 | -1483 | 131 |
| 816 | S256 | -1497 | 236 |
| 817 | S255 | -1511 | 131 |
| 818 | S254 | -1525 | 236 |
| 819 | S253 | -1539 | 131 |
| 820 | S252 | -1553 | 236 |
| 821 | S251 | -1567 | 131 |
| 822 | S250 | -1581 | 236 |
| 823 | S249 | -1595 | 131 |
| 824 | S248 | -1609 | 236 |
| 825 | S247 | -1623 | 131 |
| 826 | S246 | -1637 | 236 |
| 827 | S245 | -1651 | 131 |
| 828 | S244 | -1665 | 236 |
| 829 | S243 | -1679 | 131 |
| 830 | S242 | -1693 | 236 |
| 831 | S241 | -1707 | 131 |
| 832 | S240 | -1721 | 236 |
| 833 | S239 | -1735 | 131 |
| 834 | S238 | -1749 | 236 |
| 835 | S237 | -1763 | 131 |
| 836 | S236 | -1777 | 236 |
| 837 | S235 | -1791 | 131 |
| 838 | S234 | -1805 | 236 |
| 839 | S233 | -1819 | 131 |
| 840 | S232 | -1833 | 236 |
| 841 | S231 | -1847 | 131 |
| 842 | S230 | -1861 | 236 |
| 843 | S229 | -1875 | 131 |
| 844 | S228 | -1889 | 236 |
| 845 | S227 | -1903 | 131 |

| PAD No. | PAD Name | X | Y |
|---|---|---|---|
| 846 | S226 | -1917 | 236 |
| 847 | S225 | -1931 | 131 |
| 848 | S224 | -1945 | 236 |
| 849 | S223 | -1959 | 131 |
| 850 | S222 | -1973 | 236 |
| 851 | S221 | -1987 | 131 |
| 852 | S220 | -2001 | 236 |
| 853 | S219 | -2015 | 131 |
| 854 | S218 | -2029 | 236 |
| 855 | S217 | -2043 | 131 |
| 856 | S216 | -2057 | 236 |
| 857 | S215 | -2071 | 131 |
| 858 | S214 | -2085 | 236 |
| 859 | S213 | -2099 | 131 |
| 860 | S212 | -2113 | 236 |
| 861 | S211 | -2127 | 131 |
| 862 | S210 | -2141 | 236 |
| 863 | S209 | -2155 | 131 |
| 864 | S208 | -2169 | 236 |
| 865 | S207 | -2183 | 131 |
| 866 | S206 | -2197 | 236 |
| 867 | S205 | -2211 | 131 |
| 868 | S204 | -2225 | 236 |
| 869 | S203 | -2239 | 131 |
| 870 | S202 | -2253 | 236 |
| 871 | S201 | -2267 | 131 |
| 872 | S200 | -2281 | 236 |
| 873 | S199 | -2295 | 131 |
| 874 | S198 | -2309 | 236 |
| 875 | S197 | -2323 | 131 |
| 876 | S196 | -2337 | 236 |
| 877 | S195 | -2351 | 131 |
| 878 | S194 | -2365 | 236 |
| 879 | S193 | -2379 | 131 |
| 880 | S192 | -2393 | 236 |
| 881 | S191 | -2407 | 131 |
| 882 | S190 | -2421 | 236 |
| 883 | S189 | -2435 | 131 |
| 884 | S188 | -2449 | 236 |
| 885 | S187 | -2463 | 131 |
| 886 | S186 | -2477 | 236 |
| 887 | S185 | -2491 | 131 |
| 888 | S184 | -2505 | 236 |
| 889 | S183 | -2519 | 131 |
| 890 | S182 | -2533 | 236 |
| 891 | S181 | -2547 | 131 |
| 892 | S180 | -2561 | 236 |
| 893 | S179 | -2575 | 131 |
| 894 | S178 | -2589 | 236 |
| 895 | S177 | -2603 | 131 |
| 896 | S176 | -2617 | 236 |
| 897 | S175 | -2631 | 131 |
| 898 | S174 | -2645 | 236 |

| PAD No. | PAD Name | X | Y |
|---|---|---|---|
| 899 | S173 | -2659 | 131 |
| 900 | S172 | -2673 | 236 |
| 901 | S171 | -2687 | 131 |
| 902 | S170 | -2701 | 236 |
| 903 | S169 | -2715 | 131 |
| 904 | S168 | -2729 | 236 |
| 905 | S167 | -2743 | 131 |
| 906 | S166 | -2757 | 236 |
| 907 | S165 | -2771 | 131 |
| 908 | S164 | -2785 | 236 |
| 909 | S163 | -2799 | 131 |
| 910 | S162 | -2813 | 236 |
| 911 | S161 | -2827 | 131 |
| 912 | S160 | -2841 | 236 |
| 913 | S159 | -2855 | 131 |
| 914 | S158 | -2869 | 236 |
| 915 | S157 | -2883 | 131 |
| 916 | S156 | -2897 | 236 |
| 917 | S155 | -2911 | 131 |
| 918 | S154 | -2925 | 236 |
| 919 | S153 | -2939 | 131 |
| 920 | S152 | -2953 | 236 |
| 921 | S151 | -2967 | 131 |
| 922 | S150 | -2981 | 236 |
| 923 | S149 | -2995 | 131 |
| 924 | S148 | -3009 | 236 |
| 925 | S147 | -3023 | 131 |
| 926 | S146 | -3037 | 236 |
| 927 | S145 | -3051 | 131 |
| 928 | S144 | -3065 | 236 |
| 929 | S143 | -3079 | 131 |
| 930 | S142 | -3093 | 236 |
| 931 | S141 | -3107 | 131 |
| 932 | S140 | -3121 | 236 |
| 933 | S139 | -3135 | 131 |
| 934 | S138 | -3149 | 236 |
| 935 | S137 | -3163 | 131 |
| 936 | S136 | -3177 | 236 |
| 937 | S135 | -3191 | 131 |
| 938 | S134 | -3205 | 236 |
| 939 | S133 | -3219 | 131 |
| 940 | S132 | -3233 | 236 |
| 941 | S131 | -3247 | 131 |
| 942 | S130 | -3261 | 236 |
| 943 | S129 | -3275 | 131 |
| 944 | S128 | -3289 | 236 |
| 945 | S127 | -3303 | 131 |
| 946 | S126 | -3317 | 236 |
| 947 | S125 | -3331 | 131 |
| 948 | S124 | -3345 | 236 |
| 949 | S123 | -3359 | 131 |
| 950 | S122 | -3373 | 236 |
| 951 | S121 | -3387 | 131 |

| PAD No. | PAD Name | X | Y |
|---|---|---|---|
| 952 | S120 | -3401 | 236 |
| 953 | S119 | -3415 | 131 |
| 954 | S118 | -3429 | 236 |
| 955 | S117 | -3443 | 131 |
| 956 | S116 | -3457 | 236 |
| 957 | S115 | -3471 | 131 |
| 958 | S114 | -3485 | 236 |
| 959 | S113 | -3499 | 131 |
| 960 | S112 | -3513 | 236 |
| 961 | S111 | -3527 | 131 |
| 962 | S110 | -3541 | 236 |
| 963 | S109 | -3555 | 131 |
| 964 | S108 | -3569 | 236 |
| 965 | S107 | -3583 | 131 |
| 966 | S106 | -3597 | 236 |
| 967 | S105 | -3611 | 131 |
| 968 | S104 | -3625 | 236 |
| 969 | S103 | -3639 | 131 |
| 970 | S102 | -3653 | 236 |
| 971 | S101 | -3667 | 131 |
| 972 | S100 | -3681 | 236 |
| 973 | S99 | -3695 | 131 |
| 974 | S98 | -3709 | 236 |
| 975 | S97 | -3723 | 131 |
| 976 | S96 | -3737 | 236 |
| 977 | S95 | -3751 | 131 |
| 978 | S94 | -3765 | 236 |
| 979 | S93 | -3779 | 131 |
| 980 | S92 | -3793 | 236 |
| 981 | S91 | -3807 | 131 |
| 982 | S90 | -3821 | 236 |
| 983 | S89 | -3835 | 131 |
| 984 | S88 | -3849 | 236 |
| 985 | S87 | -3863 | 131 |
| 986 | S86 | -3877 | 236 |
| 987 | S85 | -3891 | 131 |
| 988 | S84 | -3905 | 236 |
| 989 | S83 | -3919 | 131 |
| 990 | S82 | -3933 | 236 |
| 991 | S81 | -3947 | 131 |
| 992 | S80 | -3961 | 236 |
| 993 | S79 | -3975 | 131 |
| 994 | S78 | -3989 | 236 |
| 995 | S77 | -4003 | 131 |
| 996 | S76 | -4017 | 236 |
| 997 | S75 | -4031 | 131 |
| 998 | S74 | -4045 | 236 |
| 999 | S73 | -4059 | 131 |
| 1000 | S72 | -4073 | 236 |
| 1001 | S71 | -4087 | 131 |
| 1002 | S70 | -4101 | 236 |
| 1003 | S69 | -4115 | 131 |
| 1004 | S68 | -4129 | 236 |

| PAD No. | PAD Name | X | Y |
|---|---|---|---|
| 1005 | S67 | -4143 | 131 |
| 1006 | S66 | -4157 | 236 |
| 1007 | S65 | -4171 | 131 |
| 1008 | S64 | -4185 | 236 |
| 1009 | S63 | -4199 | 131 |
| 1010 | S62 | -4213 | 236 |
| 1011 | S61 | -4227 | 131 |
| 1012 | S60 | -4241 | 236 |
| 1013 | S59 | -4255 | 131 |
| 1014 | S58 | -4269 | 236 |
| 1015 | S57 | -4283 | 131 |
| 1016 | S56 | -4297 | 236 |
| 1017 | S55 | -4311 | 131 |
| 1018 | S54 | -4325 | 236 |
| 1019 | S53 | -4339 | 131 |
| 1020 | S52 | -4353 | 236 |
| 1021 | S51 | -4367 | 131 |
| 1022 | S50 | -4381 | 236 |
| 1023 | S49 | -4395 | 131 |
| 1024 | S48 | -4409 | 236 |
| 1025 | S47 | -4423 | 131 |
| 1026 | S46 | -4437 | 236 |
| 1027 | S45 | -4451 | 131 |
| 1028 | S44 | -4465 | 236 |
| 1029 | S43 | -4479 | 131 |
| 1030 | S42 | -4493 | 236 |
| 1031 | S41 | -4507 | 131 |
| 1032 | S40 | -4521 | 236 |
| 1033 | S39 | -4535 | 131 |
| 1034 | S38 | -4549 | 236 |
| 1035 | S37 | -4563 | 131 |
| 1036 | S36 | -4577 | 236 |
| 1037 | S35 | -4591 | 131 |
| 1038 | S34 | -4605 | 236 |
| 1039 | S33 | -4619 | 131 |
| 1040 | S32 | -4633 | 236 |
| 1041 | S31 | -4647 | 131 |
| 1042 | S30 | -4661 | 236 |
| 1043 | S29 | -4675 | 131 |
| 1044 | S28 | -4689 | 236 |
| 1045 | S27 | -4703 | 131 |
| 1046 | S26 | -4717 | 236 |
| 1047 | S25 | -4731 | 131 |
| 1048 | S24 | -4745 | 236 |
| 1049 | S23 | -4759 | 131 |
| 1050 | S22 | -4773 | 236 |
| 1051 | S21 | -4787 | 131 |
| 1052 | S20 | -4801 | 236 |
| 1053 | S19 | -4815 | 131 |
| 1054 | S18 | -4829 | 236 |
| 1055 | S17 | -4843 | 131 |
| 1056 | S16 | -4857 | 236 |
| 1057 | S15 | -4871 | 131 |

| PAD No. | PAD Name | X | Y |
|---|---|---|---|
| 1058 | S14 | -4885 | 236 |
| 1059 | S13 | -4899 | 131 |
| 1060 | S12 | -4913 | 236 |
| 1061 | S11 | -4927 | 131 |
| 1062 | S10 | -4941 | 236 |
| 1063 | S9 | -4955 | 131 |
| 1064 | S8 | -4969 | 236 |
| 1065 | S7 | -4983 | 131 |
| 1066 | S6 | -4997 | 236 |
| 1067 | S5 | -5011 | 131 |
| 1068 | S4 | -5025 | 236 |
| 1069 | S3 | -5039 | 131 |
| 1070 | S2 | -5053 | 236 |
| 1071 | S1 | -5067 | 131 |
| 1072 | DUMMY9 | -5081 | 236 |
| 1073 | DUMMY10 | -5135 | 236 |
| 1074 | G1 | -5149 | 131 |
| 1075 | G3 | -5163 | 236 |
| 1076 | G5 | -5177 | 131 |
| 1077 | G7 | -5191 | 236 |
| 1078 | G9 | -5205 | 131 |
| 1079 | G11 | -5219 | 236 |
| 1080 | G13 | -5233 | 131 |
| 1081 | G15 | -5247 | 236 |
| 1082 | G17 | -5261 | 131 |
| 1083 | G19 | -5275 | 236 |
| 1084 | G21 | -5289 | 131 |
| 1085 | G23 | -5303 | 236 |
| 1086 | G25 | -5317 | 131 |
| 1087 | G27 | -5331 | 236 |
| 1088 | G29 | -5345 | 131 |
| 1089 | G31 | -5359 | 236 |
| 1090 | G33 | -5373 | 131 |
| 1091 | G35 | -5387 | 236 |
| 1092 | G37 | -5401 | 131 |
| 1093 | G39 | -5415 | 236 |
| 1094 | G41 | -5429 | 131 |
| 1095 | G43 | -5443 | 236 |
| 1096 | G45 | -5457 | 131 |
| 1097 | G47 | -5471 | 236 |
| 1098 | G49 | -5485 | 131 |
| 1099 | G51 | -5499 | 236 |
| 1100 | G53 | -5513 | 131 |
| 1101 | G55 | -5527 | 236 |
| 1102 | G57 | -5541 | 131 |
| 1103 | G59 | -5555 | 236 |
| 1104 | G61 | -5569 | 131 |
| 1105 | G63 | -5583 | 236 |
| 1106 | G65 | -5597 | 131 |
| 1107 | G67 | -5611 | 236 |
| 1108 | G69 | -5625 | 131 |
| 1109 | G71 | -5639 | 236 |
| 1110 | G73 | -5653 | 131 |

| PAD No. | PAD Name | X | Y |
|---|---|---|---|
| 1111 | G75 | -5667 | 236 |
| 1112 | G77 | -5681 | 131 |
| 1113 | G79 | -5695 | 236 |
| 1114 | G81 | -5709 | 131 |
| 1115 | G83 | -5723 | 236 |
| 1116 | G85 | -5737 | 131 |
| 1117 | G87 | -5751 | 236 |
| 1118 | G89 | -5765 | 131 |
| 1119 | G91 | -5779 | 236 |
| 1120 | G93 | -5793 | 131 |
| 1121 | G95 | -5807 | 236 |
| 1122 | G97 | -5821 | 131 |
| 1123 | G99 | -5835 | 236 |
| 1124 | G101 | -5849 | 131 |
| 1125 | G103 | -5863 | 236 |
| 1126 | G105 | -5877 | 131 |
| 1127 | G107 | -5891 | 236 |
| 1128 | G109 | -5905 | 131 |
| 1129 | G111 | -5919 | 236 |
| 1130 | G113 | -5933 | 131 |
| 1131 | G115 | -5947 | 236 |
| 1132 | G117 | -5961 | 131 |
| 1133 | G119 | -5975 | 236 |
| 1134 | G121 | -5989 | 131 |
| 1135 | G123 | -6003 | 236 |
| 1136 | G125 | -6017 | 131 |
| 1137 | G127 | -6031 | 236 |
| 1138 | G129 | -6045 | 131 |
| 1139 | G131 | -6059 | 236 |
| 1140 | G133 | -6073 | 131 |
| 1141 | G135 | -6087 | 236 |
| 1142 | G137 | -6101 | 131 |
| 1143 | G139 | -6115 | 236 |
| 1144 | G141 | -6129 | 131 |
| 1145 | G143 | -6143 | 236 |
| 1146 | G145 | -6157 | 131 |
| 1147 | G147 | -6171 | 236 |
| 1148 | G149 | -6185 | 131 |
| 1149 | G151 | -6199 | 236 |
| 1150 | G153 | -6213 | 131 |
| 1151 | G155 | -6227 | 236 |
| 1152 | G157 | -6241 | 131 |
| 1153 | G159 | -6255 | 236 |

| PAD No. | PAD Name | X | Y |
|---|---|---|---|
| 1154 | G161 | -6269 | 131 |
| 1155 | G163 | -6283 | 236 |
| 1156 | G165 | -6297 | 131 |
| 1157 | G167 | -6311 | 236 |
| 1158 | G169 | -6325 | 131 |
| 1159 | G171 | -6339 | 236 |
| 1160 | G173 | -6353 | 131 |
| 1161 | G175 | -6367 | 236 |
| 1162 | G177 | -6381 | 131 |
| 1163 | G179 | -6395 | 236 |
| 1164 | G181 | -6409 | 131 |
| 1165 | G183 | -6423 | 236 |
| 1166 | G185 | -6437 | 131 |
| 1167 | G187 | -6451 | 236 |
| 1168 | G189 | -6465 | 131 |
| 1169 | G191 | -6479 | 236 |
| 1170 | G193 | -6493 | 131 |
| 1171 | G195 | -6507 | 236 |
| 1172 | G197 | -6521 | 131 |
| 1173 | G199 | -6535 | 236 |
| 1174 | G201 | -6549 | 131 |
| 1175 | G203 | -6563 | 236 |
| 1176 | G205 | -6577 | 131 |
| 1177 | G207 | -6591 | 236 |
| 1178 | G209 | -6605 | 131 |
| 1179 | G211 | -6619 | 236 |
| 1180 | G213 | -6633 | 131 |
| 1181 | G215 | -6647 | 236 |
| 1182 | G217 | -6661 | 131 |
| 1183 | G219 | -6675 | 236 |
| 1184 | G221 | -6689 | 131 |
| 1185 | G223 | -6703 | 236 |
| 1186 | G225 | -6717 | 131 |
| 1187 | G227 | -6731 | 236 |
| 1188 | G229 | -6745 | 131 |
| 1189 | G231 | -6759 | 236 |
| 1190 | G233 | -6773 | 131 |
| 1191 | G235 | -6787 | 236 |
| 1192 | G237 | -6801 | 131 |
| 1193 | G239 | -6815 | 236 |
| 1194 | G241 | -6829 | 131 |
| 1195 | G243 | -6843 | 236 |
| 1196 | G245 | -6857 | 131 |

| PAD No. | PAD Name | X | Y |
|---|---|---|---|
| 1197 | G247 | -6871 | 236 |
| 1198 | G249 | -6885 | 131 |
| 1199 | G251 | -6899 | 236 |
| 1200 | G253 | -6913 | 131 |
| 1201 | G255 | -6927 | 236 |
| 1202 | G257 | -6941 | 131 |
| 1203 | G259 | -6955 | 236 |
| 1204 | G261 | -6969 | 131 |
| 1205 | G263 | -6983 | 236 |
| 1206 | G265 | -6997 | 131 |
| 1207 | G267 | -7011 | 236 |
| 1208 | G269 | -7025 | 131 |
| 1209 | G271 | -7039 | 236 |
| 1210 | G273 | -7053 | 131 |
| 1211 | G275 | -7067 | 236 |
| 1212 | G277 | -7081 | 131 |
| 1213 | G279 | -7095 | 236 |
| 1214 | G281 | -7109 | 131 |
| 1215 | G283 | -7123 | 236 |
| 1216 | G285 | -7137 | 131 |
| 1217 | G287 | -7151 | 236 |
| 1218 | G289 | -7165 | 131 |
| 1219 | G291 | -7179 | 236 |
| 1220 | G293 | -7193 | 131 |
| 1221 | G295 | -7207 | 236 |
| 1222 | G297 | -7221 | 131 |
| 1223 | G299 | -7235 | 236 |
| 1224 | G301 | -7249 | 131 |
| 1225 | G303 | -7263 | 236 |
| 1226 | G305 | -7277 | 131 |
| 1227 | G307 | -7291 | 236 |
| 1228 | G309 | -7305 | 131 |
| 1229 | G311 | -7319 | 236 |
| 1230 | G313 | -7333 | 131 |
| 1231 | G315 | -7347 | 236 |
| 1232 | G317 | -7361 | 131 |
| 1233 | G319 | -7375 | 236 |
| 1234 | DUMMY11 | -7389 | 131 |
| 1235 | DUMMY12 | -7403 | 236 |

### 9.5. Alignment Mark

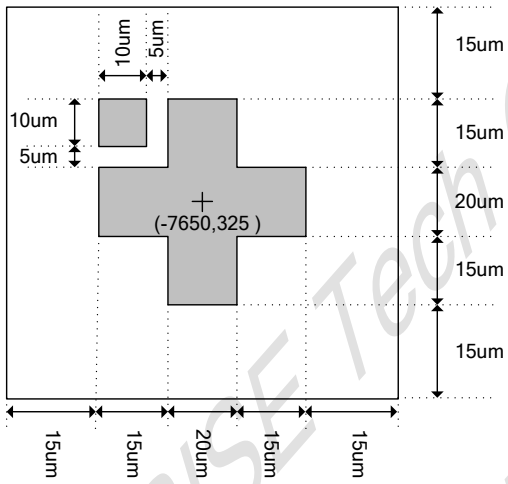
--Alignment Mark coordinate

Left (-7480, 238.5)

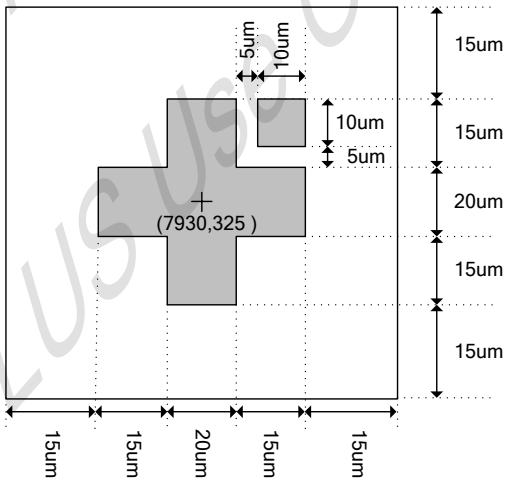
Right (7480, 238.5)

--Alignment Mark size

Left




Right



### 9.6. Wiring Resistance

| | Name | Wiring Resistance | | Name | Wiring Resistance | | Name | Wiring Resistance |
|---|---|---|---|---|---|---|---|---|
| 1 | DUMMY1 | Open | 72 | VCL | 15 ohm | 143 | D13 | 100 ohm |
| 2 | VCOM | 10 ohm | 73 | VCL | | 144 | D12 | 100 ohm |
| 3 | VCOM | | 74 | VCL | | 145 | D11 | 100 ohm |
| 4 | VCOM | | 75 | VCL | | 146 | D10 | 100 ohm |
| 5 | VCOM | | 76 | VCL | | 147 | D9 | 100 ohm |
| 6 | VCOM | | 77 | VCL | | 148 | D8 | 100 ohm |
| 7 | TEST1 | 100 ohm | 78 | C1M | 10 ohm | 149 | TEST3 | 100 ohm |
| 8 | BC | 100 ohm | 79 | C1M | | 150 | TEST4 | 100 ohm |
| 9 | BC | | 80 | C1M | | 151 | TEST5 | 100 ohm |
| 10 | VSSA | 15 ohm | 81 | C1M | | 152 | TEST6 | 100 ohm |
| 11 | VSSA | | 82 | C1M | | 153 | TEST7 | 100 ohm |
| 12 | VCOML | 20 ohm | 83 | C1M | | 154 | TEST8 | 100 ohm |
| 13 | VCOMH | 25 ohm | 84 | C1P | 10 ohm | 155 | TEST9 | 100 ohm |
| 14 | GVDD | 30 ohm | 85 | C1P | | 156 | TEST10 | 100 ohm |
| 15 | VSSA | 15 ohm | 86 | C1P | | 157 | VSS | note 1 |
| 16 | VSSA | | 87 | C1P | | 158 | IM3 | 100 ohm |
| 17 | VSSA | | 88 | C1P | | 159 | IM2 | 100 ohm |
| 18 | VSSA | | 89 | C1P | | 160 | IM1 | 100 ohm |
| 19 | VSSA | | 90 | VDDA | 10 ohm | 161 | IM0 | 100 ohm |
| 20 | VSSA | | 91 | VDDA | | 162 | VDDIO | note 1 |
| 21 | VSSA | | 92 | VDDA | | 163 | VREF | 20 ohm |
| 22 | C3M | 25 ohm | 93 | VDDA | | 164 | VDD_18V | 20 ohm |
| 23 | C3M | | 94 | VDDA | | 165 | VDD_18V | |
| 24 | C3M | | 95 | VDDA | | 166 | VDD_18V | |
| 25 | C3P | 25 ohm | 96 | VCI1 | 100 ohm | 167 | VDD_18V | |
| 26 | C3P | | 97 | TEST2 | 100 ohm | 168 | VDD_18V | |
| 27 | C3P | | 98 | CSX | 100 ohm | 169 | VSS | 10 ohm |
| 28 | C4M | 25 ohm | 99 | RDX | 100 ohm | 170 | VSS | |
| 29 | C4M | | 100 | TE | 100 ohm | 171 | VSS | |
| 30 | C4M | | 101 | WRX | 100 ohm | 172 | VSS | |
| 31 | C4P | 25 ohm | 102 | DCX | 100 ohm | 173 | VSS | |
| 32 | C4P | | 103 | VDD_OTP | 25 ohm | 174 | VSS | |
| 33 | C4P | | 104 | VDD_OTP | | 175 | VSS | |
| 34 | VGH | 15 ohm | 105 | VDD_OTP | | 176 | TEST11 | 100 ohm |
| 35 | VGH | | 106 | VDDIO | 25 ohm | 177 | TEST12 | 100 ohm |
| 36 | VGH | | 107 | VDDIO | | 178 | VSSA | 15 ohm |
| 37 | VGH | | 108 | VDDIO | | 179 | VSSA | |
| 38 | VGL | 15 ohm | 109 | VDDIO | | 180 | VCOM | 10 ohm |
| 39 | VGL | | 110 | VDDIO | | 181 | VCOM | |
| 40 | VGL | | 111 | VDD_BC | 25 ohm | 182 | VCOM | |
| 41 | VGL | | 112 | VDD | 10 ohm | 183 | VCOM | |
| 42 | VGL | | 113 | VDD | | 184 | VCOM | |
| 43 | C5P | 15 ohm | 114 | VDD | | 185 | DUMMY2 | Open |
| 44 | C5P | | 115 | VDD | | | | |
| 45 | C5P | | 116 | VDD | | | | |
| 46 | C5P | | 117 | VDD | | | | |
| 47 | C5P | | 118 | VDD | | | | |
| 48 | C5M | 15 ohm | 119 | VDD | | | | |
| 49 | C5M | | 120 | VDD | | | | |
| 50 | C5M | | 121 | VDD | | | | |
| 51 | C5M | | 122 | VDD | | | | |
| 52 | C5M | | 123 | VSS | note 1 | | | |
| 53 | VSS | 10 ohm | 124 | RESX | 100 ohm | | | |
| 54 | VSS | | 125 | RESX | | | | |
| 55 | VSS | | 126 | EXTC | 100 ohm | | | |
| 56 | VSS | | 127 | D7 | 100 ohm | | | |
| 57 | VSS | | 128 | D6 | 100 ohm | | | |
| 58 | VSS | | 129 | D5 | 100 ohm | | | |
| 59 | VSS | | 130 | D4 | 100 ohm | | | |
| 60 | C2M | 20 ohm | 131 | VSS | note 1 | | | |
| 61 | C2M | | 132 | D3 | 100 ohm | | | |
| 62 | C2M | | 133 | D2 | 100 ohm | | | |
| 63 | C2M | | 134 | D1 | 100 ohm | | | |
| 64 | C2M | | 135 | D0 | 100 ohm | | | |
| 65 | C2M | | 136 | VSS | note 1 | | | |
| 66 | C2P | 20 ohm | 137 | SDA | 100 ohm | | | |
| 67 | C2P | | 138 | SDA | | | | |
| 68 | C2P | | 139 | D17 | 100 ohm | | | |
| 69 | C2P | | 140 | D16 | 100 ohm | | | |
| 70 | C2P | | 141 | D15 | 100 ohm | | | |
| 71 | C2P | | 142 | D14 | 100 ohm | | | |

note1: These "VSS" and "VDDIO" pins can be open or connected to neighbor option pins to become pull-up or pull-down power/ground source.

note2: If user don't use CABC function, please let the BC open. If user want to use CABC, this pin will become the output of back light control signal.

## 10. COG PRODUCTS MANUFACTURING GUIDELINES

### 10.1. Purpose:

The purpose of this specification is to identify ACF bonding process, so that customers can use properly ACF and Chip during the assembly.

### 10.2. Scope:

#### 10.2.1. ACF bonding process

### 10.3. Noun definition

#### 10.3.1. COG: Chip on Glass

#### 10.3.2. ACF (Anisotropic Cunductive Film): .ACF is a functional adhesive tape which is able to connect (conductivity, adhesion, insulation) multiterminals in one time.

#### 10.3.3. CTE: Coefficient of thermal expansion

### 10.4. Responsibility unity:

ORISETECH Quality Assurance unity

### 10.5. Contents:

#### 10.5.1. Applicable documents

IPC-SM-782: Surface Mount Design & Land Pattern Standard

IPC-7351Generic Requirements for Surface Mount Design and Land Pattern Standard.

IPC JEDEC: J-STD-033A Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

JESD22-B111: Board Level Drop Test of Components for Handheld Electronic Products

IPC-A-610: Acceptability of Electronic Assemblies

#### 10.5.2. ACF Characteristics:

10.5.2.1. Three factors to achieve the connection: Temperature, Pressure, Time.

#### 10.5.3. ACF process :

10.5.3.1. To use Low Temperature and Low stress ACF is recommended for thin chip as 300 um.

10.5.3.2. Warp issues may happen if customers do not use Low Temperature and Low stress ACF for long chip .And warp issues may induce chip broken after ACF bonding for the CTE mismatch of Glass and ACF and Chip.

10.5.3.3. To use 3um ACF is recommended for BUMP space is less than 13um.

10.5.3.4. To use Low temperature and long time bonding is recommended if delamination happens in edge of chip.

10.5.3.5. For fine pitch and thin chip (300 um) products, customer should review ACF bonding condition with ACF maker.

### 10.6. References:

*IPC:

http://www.ipc.org

*HDPUG (High Density Package Users Group)

http://www.hdpug.org

*JEDEC (Joint Electronic Device Engineering Council)

http://www.jedec.org

*JEITA (Japan Electronic Industry Association)

http://www.jeita.org

## 11. DISCLAIMER

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## 12. REVISION HISTORY

| Date | Revision # | Description | Page |
|---|---|---|---|
| MAR. 27, 2009 | 0.5 | 1. Modify command DE | 17,104 |
| | | 2. Add command CB | 16,94 |
| | | 3. Add command CB | 16,95 |
| | | 4. Modify the maximum wiring resistance | 183 |
| MAR. 13, 2009 | 0.4 | 1. Modify the dimension of bump. | 171 |
| | | 2. Modify the ratio setting of pump. | 87 |
| | | 3. Modify Command B6 | 16, 81 |
| | | 4. Delete default table | 106, 107 |
| | | 5. Modify default table (C0,C5,C6) | 85,91,93 |
| | | 6. Modify 9.1 PAD Assignment | 170 |
| JAN. 05, 2009 | 0.3 | 1. Add command BA in Command list | 15 |
| | | 2. Modify Command list (2)(3)(4)(5) | 15~17 |
| | | 3. Delete Command list (6) (7) (8) (9) | 17~19 |
| | | 4. Modify Command B1 | 79 |
| | | 5. Modify Command B6 | 82 |
| | | 6. Add command BA | 83 |
| | | 7. Modify Command C0 Description | 84 |
| | | 8. Modify Command C4, C5 Description | 88~92 |
| | | 9. Modify Command DF Description | 102 |
| | | 10. Delete Command E2,E3,E4,E5 | 106~114 |
| | | 11. Add PAD Assignment. | 170 |
| | | 12. Update PAD Dimension and Bump Characteristics. | 170-171 |
| DEC. 02, 2008 | 0.2 | Modify PAD Dimension. | 177 |
| NOV. 18, 2008 | 0.1 | Original | 191 |